Optimized DSP Software • Independent DSP Analysis

Comparing FPGAs and DSPs for Embedded Signal Processing

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About BDTI

ANALYSIS

- Evaluation of processors' DSP performance and capabilities
- Advisory and consulting services
- Technical publications
- Technical training
- Custom benchmarking

DEVELOPMENT

- Implementation of optimized DSP application software
- Implementation of optimized DSP software libraries
- Algorithm development

Presentation Outline

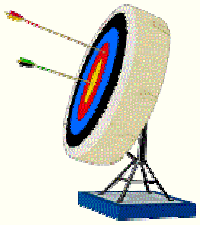
What are the driving applications?

How are DSPs meeting application needs?

Why consider FPGAs?

How do DSPs and FPGAs stack up in terms of performance?

What other factors influence designers' decisions?



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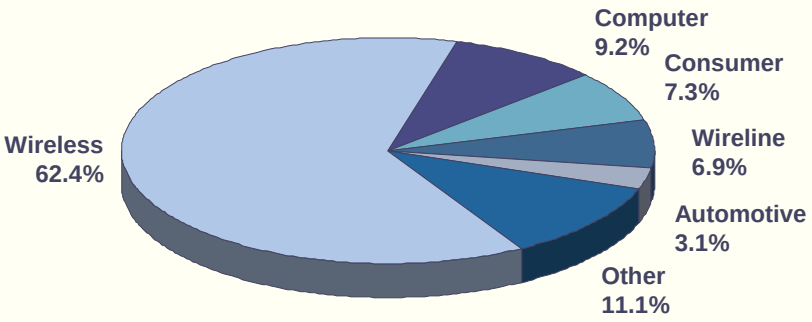
Communications: The "Killer App"



Programmable DSP Revenues by Market, Jan-Aug 2002
2002 Revenues: $4.5 Billion (Projected)

 Source: Forward Concepts 4

Comms Apps: Two Types

Infrastructure
- Wired
  - E.g., xDSL, "cable," VoIP gateway
- Wireless
  - E.g., cellular, PCS, fixed wireless, satellite

Terminals
- Portable
  - Battery-powered, size-constrained
- Non-portable (e.g., "CPE")

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Terminal Requirements

Key criteria
- Sufficient performance
- Cost
- Energy efficiency
- Memory use
- Small-system integration support
- Packaging
- Tools
- Application-development infrastructure
- Chip-product roadmap

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Infrastructure Requirements

Key criteria

- Board area per channel
- Power per channel
- Cost per channel
- Large-system integration support
- Tools
- Application-development infrastructure
- Architecture roadmap

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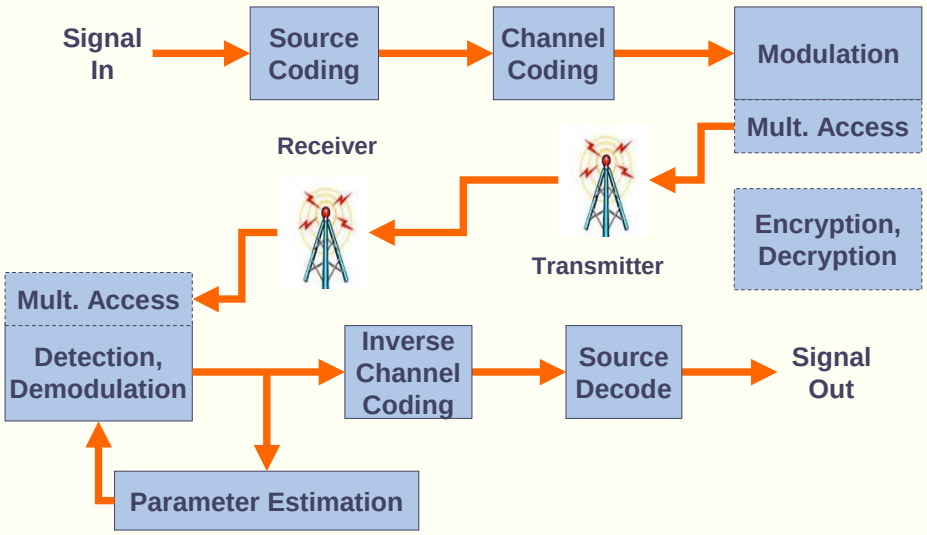
Generalized Comm System



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Key Processing Technologies

DSPs

GPPs/DSP-enhanced GPPs

Reconfigurable architectures
- FPGAs
- Reconfigurable processors

Massively parallel processors

ASSPs

ASICs
- Licensable cores
- Customizable cores
- Platform-based design

DSPs: The Incumbents

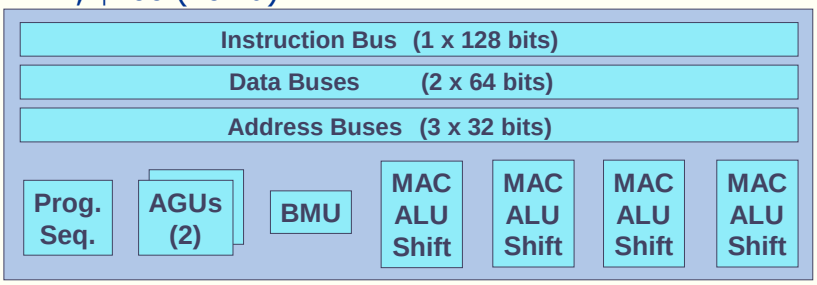
Modern conventional DSPs introduced ~1986
- One instruction, one MAC per cycle
- Developed primarily for telecom applications

High-performance VLIW DSPs introduced ~1997
- Developed primarily for wireless infrastructure
- Speed focused:
  - Independent execution units support many instructions, MACs per cycle
  - Deeper pipelines and simpler instruction sets support higher clock rates
- Emphasis on compilability

Example: StarCore SC140

Motorola, Agere,… and now Infineon

- 6-issue 16-bit fixed-point architecture
  - Up to four 16-bit MACs per cycle
- Motorola MSC8101 (one SC140 core) shipping at 300 MHz, $134 (10 ku)
- Agere SP2000B (three SC140 cores) sampling at 250 MHz, $200 (10 ku)



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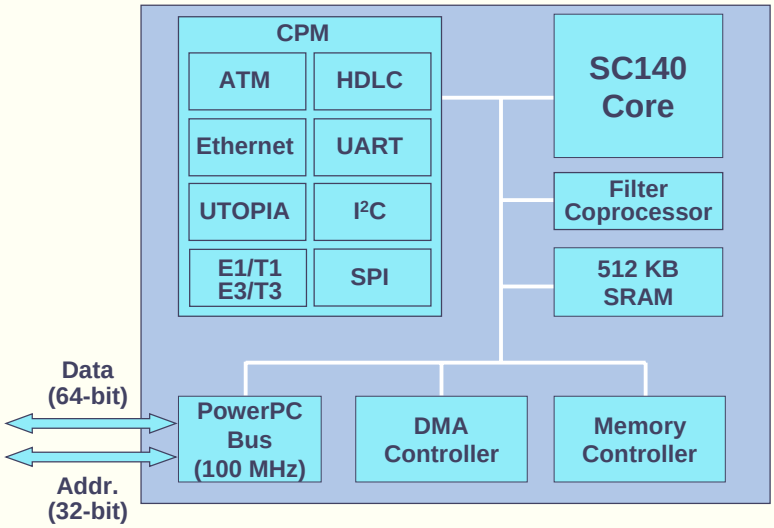
Motorola MSC8101



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Other Infrastructure DSPs

Texas Instruments TMS320C64xx
- 8-issue 16-bit fixed-point architecture
  - Up to four 16-bit MACs per cycle
  - Special instructions and co-processors for communications applications
  - Compatible with 'C62xx, 'C67xx
- Sampling at 600 MHz, $111 (10 ku)

Analog Devices TigerSHARC
- 4-issue fixed- and floating-point
  - Up to eight 16-bit fixed-point MACs per cycle
  - Special instructions for 3G base stations
  - High memory bandwidth (8 GB/s)
- Shipping at 250 MHz, $175 (10 ku)

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DSP Processors

Strengths and Weaknesses

- ↑ DSP performance, efficiency strong compared to other off-the-shelf processors
- ↓ But may not be adequate for demanding tasks
- ↑ Relatively easy to program
  - ↓ But compilers are often inefficient
  - ↓ And 'C6xxx processors are assembly programmer's worst nightmare
- ↑ Good DSP-oriented dev. tools, infrastructure
  - ↑ TI's dev. infrastructure is particularly good
  - ↓ But mediocre dev. infrastructure for non-DSP tasks

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DSP Processors

Strengths and Weaknesses

- ↑ Relatively low development cost, risk
  - ↑ Mature technology
  - ↑ Large, experienced developer base
  - ↑ Fast time-to-market
  - ↑ Some architectures available from multiple vendors
  - ↓ But some vendors' roadmaps are unclear
- ↓ Relatively limited product offerings
  - ↑ But products offer strong, relevant integration

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Wireless Bandwidth Growth

2G	2.5G	3G
• GSM	• GPRS	• 3GPP-DS-FDD
• DSC1800	• HCSD	• 3GPP-DS-TDD
• PCS1900	• IS-95C	• 3GPP-MC
• IS-95B	• IS-136+	• ARIB W-CDMA
• IS-54B	• IS-136 HS	• IS-2000 CDMA
• IS-136	• Compact EDGE	• IS-95-HDR
• PDC		
8-13 Kbps	**64-384 Kbps**	**384-2000+ Kbps**
NARROWBAND CIRCUIT VOICE		**WIDEBAND PACKET DATA**
~100 MIPS →	**~10,000 MIPS** →	**~100,000 MIPS**

 Source: MorphICs Technology, Inc. 16

Why Consider FPGAs?

"As the industry shifts from second-generation, 2G, to 3G wireless we see the percentage of the physical layer MIPS that reside in the DSP dropping from essentially 100 percent in today's technology for GSM *to about 10 percent* for wideband code-division multiple access (WCDMA)."

Texas Instruments
IEEE Communications Magazine
January 2000

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FPGAs

Field-Programmable Gate Arrays

An amorphous "sea" of reconfigurable logic with reconfigurable interconnect
- Possibly interspersed with fixed-logic resources, e.g., processors, multipliers

Potential for very high parallelism

Historically used for prototyping and "glue logic," but becoming more sophisticated
- DSP-oriented architecture features
- DSP-oriented tools and design libraries
  - Viterbi, Turbo, and Reed-Solomon coders and decoders, FIR filters, FFTs,…

Key DSP players: Altera and Xilinx

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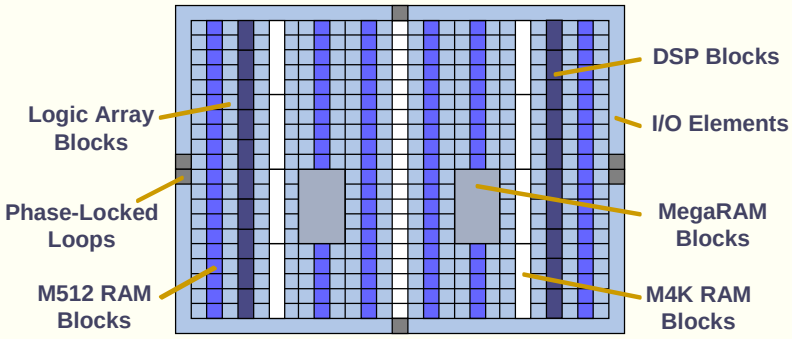
Example: Altera Stratix

Up to 28 hard-wired "DSP blocks"

- 8x9-bit, 4x18-bit, 1x36-bit multiply operations
- Optional pipelining, accumulation, etc.

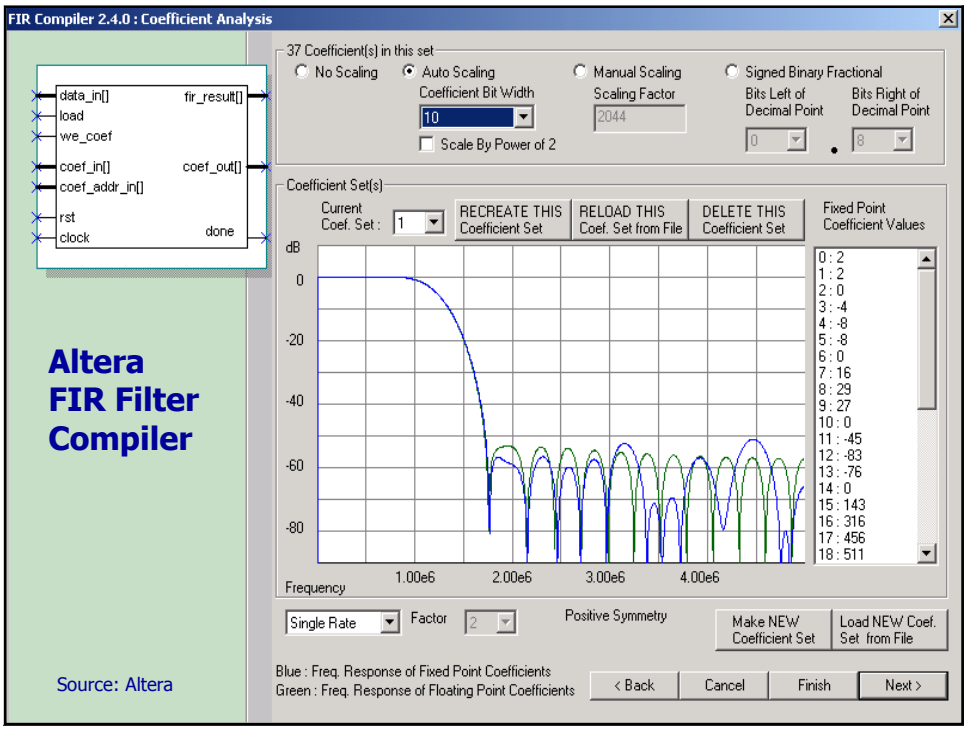
3 sizes of hard-wired memory blocks



Altera Stratix

High-end, DSP-enhanced FPGAs

- IP blocks
  - Filters, FFTs, Viterbi decoders,…
  - Nios processor
  - Third-party IP, e.g., DMA controllers
- DSP tools
  - Parameterized IP block generators
  - Simulink to FPGA link
  - C+Simulink to FPGA design flow
- Sampling now; production end of 2002
- Prices begin at $170 (1 ku)



Others: Xilinx

"Virtex" line of FPGAs

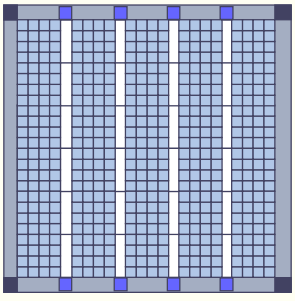
Virtex-II

- Includes array of hard-wired 18 × 18 multipliers plus distributed memory
- Up to 168 multipliers in biggest chip
- Most versions available now

Virtex-II Pro: joint effort with IBM

- Adds up to four hard-wired PowerPC 405 cores
- Up to 216 multipliers in biggest chip
- Sampling now

Prices begin at $169 (1 ku)



Source: Xilinx

FPGAs

Strengths and Weaknesses

- ↑ Massive performance gains on some algorithms
- ↑ Architectural flexibility can yield efficiency
  - ↑ Adjust data widths throughout algorithm
  - ↑ Parallelism where you need it
  - ↑ Massive on-chip memory bandwidth
- ↓ Efficiency compromised by generality
  - Embedded MAC units and memory blocks improve efficiency but reduce generality
- ↑ Re-use hardware for multiple tasks
- ↑ Field reconfigurability (for some products)

FPGAs

Strengths and Weaknesses

- ↑ Potentially good cost and power efficiency
  - ↓ But prices and power consumption are much higher than DSPs'
- ↓ Development is long and complicated
  - ↓ Design flow is unfamiliar to most DSP engineers
  - ↑ But cost and complexity is much lower than ASICs'
  - ↑ And processor cores reduce development burden
- ↓ Development infrastructure badly lags DSPs'
  - ↓ DSP-oriented tools are immature
- Xilinx has mature products, but others are playing catch-up

Performance Analysis

- Comparing performance of off-the-shelf DSP to that of FPGAs is tricky
- Common MMACS metric is oversimplified to the point of absurdity
  - FPGAs vendors use distributed-arithmetic benchmark implementations that require fixed coefficients
  - MMACS metric overlooks need to dedicate resources to non-MAC tasks
  - Many important DSP algorithms don't use MACs at all!

Alternative Approach: Application Benchmarks

Use a full application, e.g., N channels of an OFDM receiver

Hazards:

- Applications tend to be ill-defined
- Hand-optimization usually required in real-world applications
  - Costly, time-consuming to implement
  - Evaluates programmer as much as processor
  - What is a "reasonable" benchmark implementation?

Solution: Simplified Application Benchmark

BDTI's benchmark is based on a simplified OFDM receiver

- Closely resembles a real-world application
- Simplified to enable optimized implementations
- Constrained to ensure consistent, reasonable implementation practices

Benchmark goals:

- Maximize the number of channels
- Minimize the cost per channel

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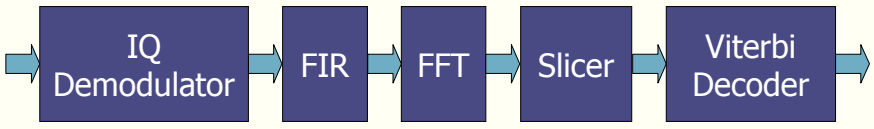
Benchmark Overview

Flexibility is an asset:

- Algorithms range from table look-ups to MAC-intensive transforms
- Data sizes range from 4 to 16 bits
- Data rates range from 40 to 320 MB/s
- Data includes real and complex values



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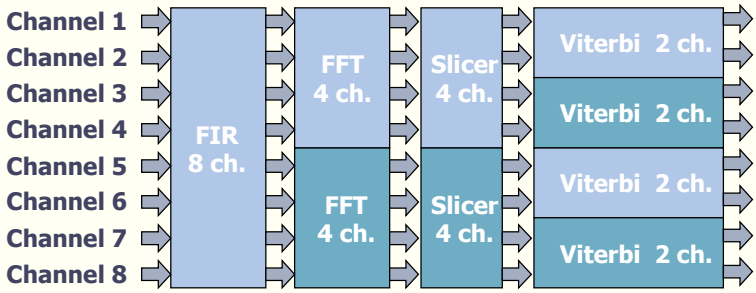
Benchmark Requirements

"Pins to pins"

Real-time throughput

Bit-exact output data

Resource sharing is permitted

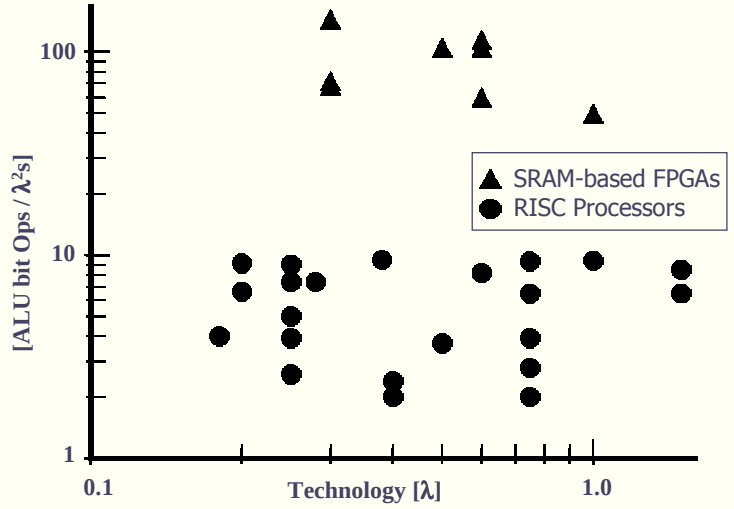


Benchmark Results

	Motorola MSC8101 (300 MHz)	Altera Stratix 1S20-6 (Projected)	Altera Stratix 1S80-6 (Preliminary)
Channels	<<1	~10	~50
Cost (1 ku)	$140	$325	$3,480
Cost per channel	~$500	~$10	~$50

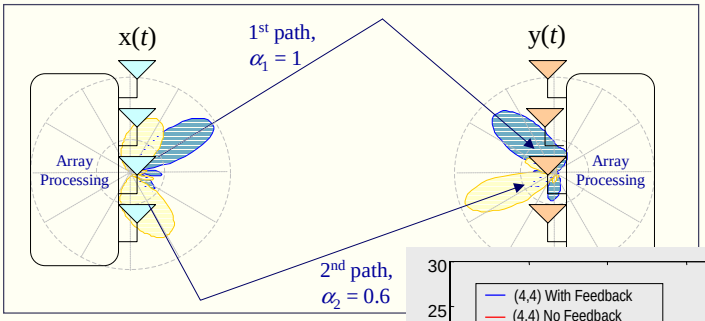
These results are approximate. For full results, see BDTI's report, *FPGAs for DSP*.

Density Comparison

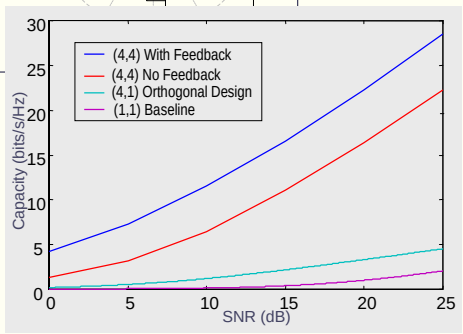


Source: Andre DeHon

Dealing with Non-Ideal Channels



Source: Jan Rabaey, Berkeley Wireless Research Center



- Multi-antenna approach exploits multi-path fading by sending data along good channels
- Results in large theoretical improvements in bandwidth efficiency for fading channels
- But…computationally hungry

Why Use a DSP?

- Many applications are not amenable to FPGA implementations
  - Parallelism is sometimes inherently limited
  - Ultimate speed is not always the first priority
- FPGAs are still too expensive for terminal applications
- FPGA energy efficiency is still an unknown
- Implementing a complex algorithm is much more difficult on an FPGA than on a DSP

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Conclusions

- High-end FPGAs can wallop DSPs on computation-intensive, highly parallelizable tasks
- FPGAs are expensive, but they can beat DSPs in terms of performance per dollar
- DSP have the advantage in development infrastructure, time-to-market,…
- The "best" architecture depends on the application
- Heterogeneous architectures, e.g., combining DSP and FPGA components, are a key trend

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For More Information…

www.BDTI.com

Free Information

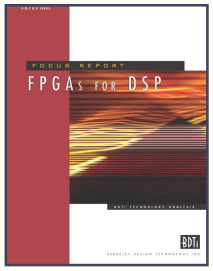
- BDTImark2000™ scores
- *DSP Insider* newsletter
- *Pocket Guide to Processors for DSP*

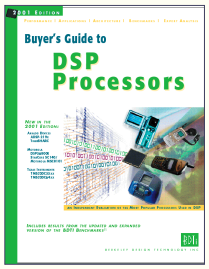
White papers on processor architectures and benchmarking

Article reprints on DSP-oriented processors and applications

- *EE Times*
- *IEEE Spectrum*
- *IEEE Computer* and others

comp.dsp FAQ





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