


Evaluating the Latest DSPs for Communications Infrastructure Applications

Optimized DSP Software • Independent DSP Analysis




Evaluating the Latest DSPs for Communications Infrastructure Applications

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Processor Requirements

Communications Infrastructure Equipment

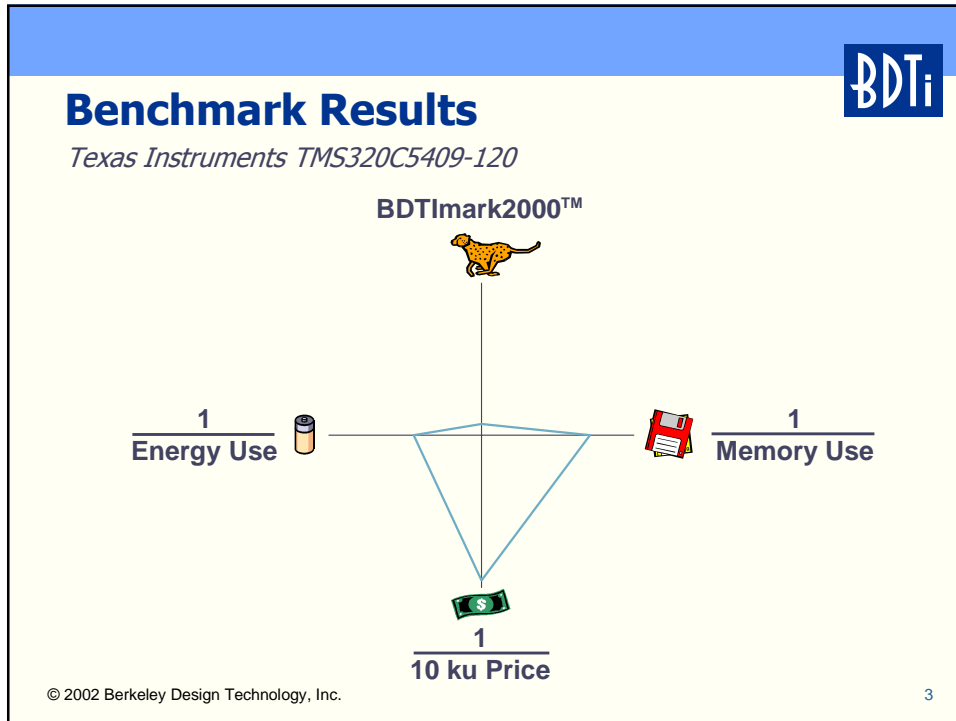
Key criteria

- Board area per channel
- Power per channel
- Cost per channel
- Large-system integration support
- Tools
- Application-development infrastructure
- Architecture roadmap

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Evaluating the Latest DSPs for Communications Infrastructure Applications



Texas Instruments TMS320C64xx

8-issue 16-bit fixed-point architecture

- Up to four 16-bit MACs per cycle
- Special instructions and co-processors for communications applications
- Compatible with 'C62xx, 'C67xx

11-stage pipeline with multicycle latencies

Two-level cache memory system

32-bit instruction set

Sampling at 600 MHz, \$111 (10 ku)

On-Chip Program Memory

Dispatch Unit


L1 S1 M1 D1 Register File A

L2 S2 M2 D2 Register File B

On-Chip Data Memory

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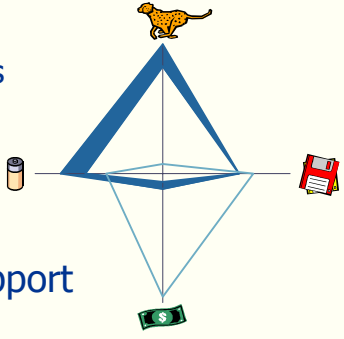
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Texas Instruments TMS320C64xx

Strengths and Weaknesses

- ↑ Good speed and cost-efficiency
 - ↓ But poor energy and memory efficiency
- ↓ Complex programming model
 - ↓ `C6xxx is assembly programmer's worst nightmare
 - ↓ Caches reduce execution-time predictability
- ↑ Good integration
- ↑ Good tools and third-party support
 - ↑ Compatible with `C6xxx family



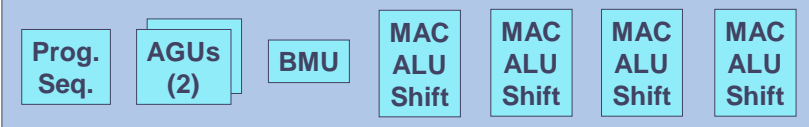
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StarCore SC140

Motorola, Agere,... and now Infineon

- 6-issue 16-bit fixed-point architecture
 - Up to four 16-bit MACs per cycle
- 5-stage pipeline with single-cycle latencies
- Some chips use caches
- Mixed-width 16- and 32-bit instruction set
- Motorola MSC8101 (one SC140 core) shipping at 300 MHz, \$134 (10 ku)
- Agere SP2000B (three SC140 cores) sampling at 250 MHz, \$200 (10 ku)



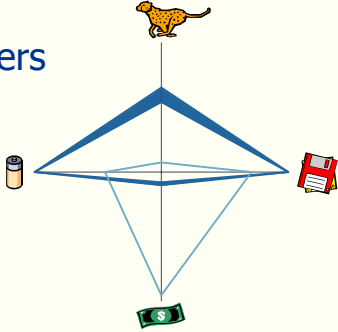
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StarCore SC140

Strengths and Weaknesses

- ↑ Strong performance on most metrics
 - ↓ But poor cost-efficiency
- ↑ Good target for compilers, assembly-language programmers
- ↑ Multi-vendor architecture
 - ↑ Backed by three of the largest semiconductor vendors
 - ↓ No roadmap or business plan from StarCore LLC
- ↑ Limited product offerings
 - ↑ Strong, relevant integration
 - ↓ But poor cost-efficiency



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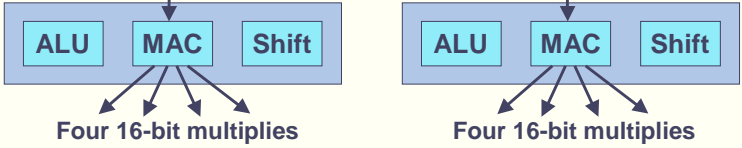
Analog Devices TigerSHARC

4-issue fixed- and floating-point hierarchal SIMD architecture

- 8-, 16-, 32-bit fixed-point and 32-bit floating-point
- Up to eight 16-bit fixed-point MACs per cycle
- Special CDMA-oriented instructions
- High memory bandwidth (8 GB/s)

Five-stage pipeline with single-cycle latencies
Shipping at 250 MHz, \$175 (10 ku)

1 SIMD multiply instruction



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Analog Devices TigerSHARC

Strengths and Weaknesses

- ↑ Speed rivals fastest fixed- and floating-point DSPs*
- ↓ Poor cost-performance*
- ↓ Two-level SIMD complicates programming
- ↑ Sophisticated memory system
 - ↑ Leading memory bandwidth
 - ↑ Excellent multiprocessor support
- ↑ Good tools
 - ↓ But limited third-party support
- ↓ Uncertain roadmap
 - ↓ Only one chip announced so far
 - ↓ Can ADI support all of its new architectures?

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LSI Logic ZSP400

A 4-Way Superscalar DSP Core

4-issue 16-bit fixed-point superscalar architecture

- Up to two 16-bit MACs per cycle
- ALUs also function as AGUs, shifters
- Good support for 32-bit operations

Five-stage pipeline with single-cycle latencies
16-bit instruction set with no conditional execution
Available as core, ASIC library component, ASSP, ...
Compatible with higher-performance ZSP G2
Shipping at 200 MHz, \$36 (10 ku)

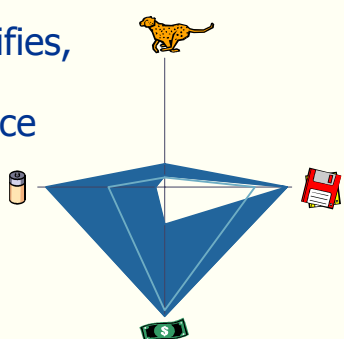
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LSI Logic ZSP400

Strengths and Weaknesses

- ↑ Cost-, energy-, and memory-efficient
 - ↓ Older chips are less cost- and energy-efficient
 - ↓ Relatively slow
- Superscalar architecture simplifies, complicates programming
- ↑ Roadmap to higher performance
- ↑ Available in multiple forms
- ↑ Acceptance appears to be growing
- ↓ Unproven tools and third-party support



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Conclusions

Developers of communications infrastructure equipment have many choices of processors.

There is no "ideal" processor:

- Any choice brings trade-offs
- The "best" processor depends on the details of the application

Performance and efficiency are key:

- Be wary of vendor hype; use reliable benchmarks

Factors other than performance are also critical:

- Vendors' roadmaps, business plans, etc.
- Tools and third-party support

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