Insight, Analysis, and Advice on Signal Processing Technology

Processors for Software-Defined Radio: Choices and Trade-offs

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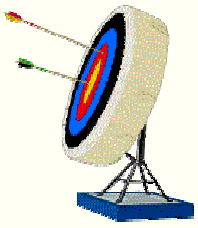
Presentation Goals

Understand key strengths and weaknesses of...
- High-end DSPs
- High-end general-purpose processors
- Signal-processing-oriented FPGAs
- Reconfigurable processors

...for signal processing in SDR applications

Understand how the options perform
- Speed
- Cost and cost-effectiveness
- Power and energy-efficiency



Programmable Signal Processing Options

DSPs

General-purpose processors (GPPs)

- **PC CPUs**
- Embedded GPPs

Reconfigurable architectures

- **FPGAs**
- **Reconfigurable processors**

DSPs: The Incumbents

Modern conventional DSPs introduced ~1986

- One instruction, one MAC per cycle
- Developed primarily for telecom applications

High-performance VLIW DSPs introduced ~1997

- Primarily targeted telecom infrastructure
- Speed focused:
  - Independent execution units support many instructions, operations per cycle
  - Deeper pipelines and simpler instruction sets support higher clock rates
- Emphasis on compilability

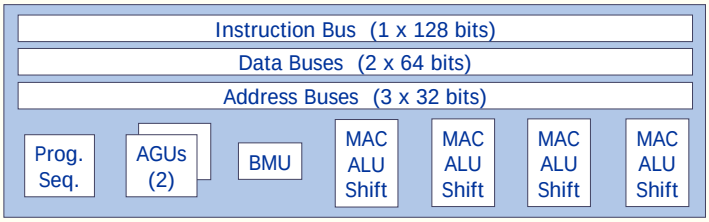
Freescale MSC711x and MSC81xx

6-issue, 16-bit fixed-point VLIW architecture
- Up to four 16-bit MACs per cycle

Mixed-width 16- and 32-bit instruction set

Mainly targeting telecom infrastructure, wireless handsets

Example parts:
- Single-core MSC7110 shipping at 200 MHz, $13 (1 ku)
- Quad-core MSC8122 sampling at 400 MHz, $171 (1 ku)



Other High-Performance DSPs

Texas Instruments TMS320C64x
- 8-issue, 16-bit fixed-point architecture
  - Up to four 16-bit MACs per cycle
  - Special instructions and co-processors for communications apps.
  - Compatible with 'C62x, 'C67x
- Example parts:
  - 'C6414T shipping at 1.0 GHz, $214 (1 ku)
  - 'C6410 shipping at 400 MHz, $20 (1 ku)

Analog Devices TigerSHARC (ADSP-TS20x)
- 4-issue fixed- and floating-point
  - Up to eight 16-bit fixed-point MACs per cycle
  - Special instructions for 3G base stations
  - High memory bandwidth (18 GB/s)
- Example parts:
  - 'TS201S shipping at 600 MHz, $242 (1 ku)
  - 'TS203S shipping at 500 MHz, $55 (1 ku)

DSP Processors

Strengths and Weaknesses

- ↑ Signal processing performance and efficiency strong vs. other types of instruction-set processors
- ↓ But may not be adequate for demanding tasks
  - ↓ Fixed architectures limit efficiency, algorithm flexibility
- ↑ Strong signal-processing-oriented tools and infrastructure
  - ↓ Sometimes, poor compiler quality
- ↑ Stable, mature technology and vendors
- ↑ Relatively low development cost, risk
- ↓ Relatively limited selection of chips for some families
  - ↑ But chips offer strong, relevant integration

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PC CPUs

High-Performance General-Purpose Processors (GPPs)

Not originally designed for signal processing, but offer:
- Very high clock rates
- Ability to execute several instructions in parallel
- Large on-chip memories on some parts

Extensive SIMD features speed signal processing
- Intel's MMX, SSE, SSE2, and SSE3
- Freescale's AltiVec

Mostly speed-focused
- Energy efficiency usually poor
- Fastest parts are very expensive

Strong emphasis on backwards compatibility

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Freescale MPC7xxx

High-End PowerPC

MPC7457 shipping at 1 GHz, ~$250 (1 ku)
- 320 Kbyte on-chip cache memory
- 20 Watt max power

MPC7410 shipping at 400 MHz, ~$50 (1 ku)
- 64 Kbyte on-chip cache memory
- 6.6 Watt max power

Extensive SIMD support
- Fixed-point: 16x8, 8x16, 4x32, 1x128
- Floating-point: 4x32

MPC74xx probably faster than any floating-point DSP
- Likely faster than most fixed-point DSPs

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PC CPUs

Strengths and Weaknesses

- ↑ Can handle substantial real-time signal-processing tasks
  - ↑ May be as fast or faster than DSP processors ...
  - ↓ ... but cost and power consumption may be higher
- ↓ Dynamic features complicate optimization, real-time
- ↓ Generally weak on integration
- ↑ Excellent targets for non-signal-processing tasks
  - ↑ E.g., packet protocol stacks
- ↑ Many options for OS, 3rd party application software
- ↑ Development tools mature, powerful
  - ↓ But typically lack signal-processing-oriented features
- ↑ Compatibility, multi-vendor architectures common
- ↓ Short life cycle for many parts

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FPGAs

Field-Programmable Gate Arrays

An amorphous "sea" of reconfigurable logic with reconfigurable interconnect
- Possibly interspersed with fixed-logic resources, e.g., processors, multipliers

Potential for very high parallelism

Historically used for prototyping and "glue logic," but now increasingly for signal processing
- DSP-oriented architecture features
- DSP-oriented tools and design libraries
  - Viterbi, Turbo, and Reed-Solomon coders and decoders, FIR filters, FFTs,...

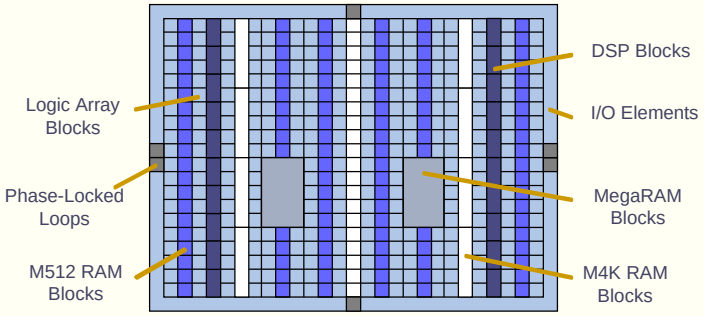
Key DSP players: Altera and Xilinx

Altera Stratix

Up to 22 hard-wired "DSP blocks"
- 8×9-bit, 4×18-bit, 1×36-bit multiply operations
- Optional pipelining, accumulation, etc.

Three sizes of hard-wired memory blocks

All announced family members are shipping now; e.g.,
- 10 Kcell version: $120 (1 ku)
- 60 Kcell version: $1,215 (1 ku)



Other High-End DSP-Oriented FPGAs

Altera Stratix II
- New logic structure uses novel 8-input logic
- Faster, less expensive, and higher capacity
- Most parts sampling now
  - 15 Kcell version: $120 (1 ku)
  - 60 Kcell version: $490 (1 ku)

Xilinx Virtex-4: three application-oriented "platforms"
- "SX" emphasizes DSP blocks, hardwired memory
  - DSP blocks consist of 18x18 multipliers plus hardware for accumulation and other operations
- "LX" emphasizes logic cells
- "FX" includes PowerPC cores
- Initial parts sampling now; 1 ku prices unavailable

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FPGAs
Strengths and Weaknesses

↑ Massive performance gains over instruction set processors on some DSP tasks
  - ↑ Huge throughput, cost/performance advantages over DSP, general-purpose processors in some applications
  - ↑ Architectural flexibility can yield efficiency
    - ↑ Adjust data widths throughout algorithm
    - ↑ Parallelism where you need it; distributed storage
    - Dynamic reconfigurability?
- ↓ High development effort compared to instruction-set processors
  - ↓ Complex design flow is unfamiliar to most signal-processing engineers
- Suitability for single-channel, low-power, cost-sensitive signal-processing applications not proven

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BDTI Communications Benchmark™

A multi-channel 10 Mbps OFDM receiver

	DSP A	DSP B	Altera Stratix 1S20-6	Altera Stratix 1S80-6
Channels	<0.2	~0.7	~20	~60
Cost (1 ku)	~$15	~$210	~$210	~$3,200
Cost per channel	~$90	~$300	~$10	~$50

From BDTI's report *FPGAs for DSP* and unpublished benchmarks.

Reconfigurable Processors

Finally Ready for Prime Time?

Goal: FPGA-like flexibility, ASIC-like efficiency, DSP processor-like programmability

Key idea: Coarse-grained reconfigurability vs. FPGA

- Pay for reconfigurability where it benefits the most

Typically an array of connected processing elements

Distributed memory provides massive bandwidth

Most are application-focused

- 3G infrastructure is the most common target

Fabless IC and core-licensing business models

Examples: Elixent, Morpho Tech, PACT, picoChip, Stretch

Reconfigurable Processors

Strengths and Weaknesses

- ↑ Potential for exceptional throughput and efficiency
  - ↑ Combination of massive parallelism **and** application-specific hardware
  - ↑ Reconfigurable processor is to FPGA as DSP is to GPP
- ↑ Potential for excellent flexibility
- ↓ Novel programming models
  - ↓ Programming models, tools immature
  - ↑ Application focus helps; e.g., software libraries, reference designs
    - ↓ But for some, the application is an afterthought
- ↓ Unproven technology, companies
  - ↓ Uncertain company, technology roadmaps

Conclusions

The good news:

- An increasingly rich field of options for high-performance, programmable signal processing
- Consistent improvement in performance, cost, energy
- SDR is possible!

The bad news:

- Nothing available today is close to an ideal solution
- The landscape is changing fast
- Difficult to make good comparisons among diverse, fast-changing options

Future Work

Further independent processor benchmarking for SDR applications is needed

- More devices: FPGAs and DSPs
- More processor types: PC CPUs and reconfigurable processors
- More metrics: energy efficiency

Additional analysis needed

- Performance isn't everything—factors such as ease of development are also critical

BDTI is pursuing new benchmarking and analysis in each of these areas

For More Information... www.BDTI.com

Inside [DSP] newsletter and quarterly reports

Benchmark scores for dozens of processors

Pocket Guide to Processors for DSP

- Basic stats on over 40 processors

Articles, white papers, and presentation slides

- Processor architectures and performance
- Signal processing applications
- Signal processing software optimization

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