Alternatives to DSP Processors for Communications Applications

Presented by
Jeff Bier
Berkeley Design Technology, Inc. (BDTI)

April 27, 2001

bier@BDTI.com
www.BDTI.com

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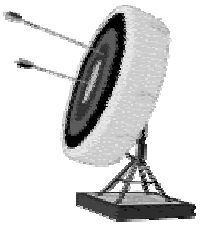
Presentation Goals

- **Why consider alternatives?**
- **What types of alternatives are relevant?**
- **Which companies are developing these?**
- **What are the major distinguishing characteristics of each type of alternative?**



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About BDTI

Independent DSP Analysis • Optimized DSP Software

- **Analytical consulting services**
- **Publications on DSP technology**
  - ***Buyer's Guide to DSP Processors***
  - ***Inside the StarCore SC140***
  - ***DSP Processor Fundamentals***
- **Training**
- **Software development services**
  - **Streaming media applications focus**

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Comms Apps: Two Types

- **Infrastructure**
  - **Wired**
    - **E.g., xDSL, "cable", VoIP gateway**
  - **Wireless**
    - **E.g., cellular, PCS, fixed wireless, satellite**
- **Terminals**
  - **Portable**
    - **Battery-powered, size-constrained**
  - **Non-portable (e.g., "CPE")**

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Infrastructure Processor Requirements

Key criteria

- **Performance/board area**
- **Performance/W**
- **Price/performance**
- **Large-system integration support**
- **Tools**
- **Application-development infrastructure**
- **Architecture roadmap**

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Terminal Processor Requirements

Key criteria

- **Energy efficiency**
- **Sufficient performance**
- **Cost**
- **Memory use**
- **Small-system integration support**
- **Tools**
- **Application-development infrastructure**
- **Packaging**
- **Chip-product roadmap**

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Why Consider Alternatives?

- **Processing throughput**
  - **3G wireless computation needs outstripping DSP processor advances**
  - **DSP processor performance gains coming at increased cost**
- **Development**
  - **DSP processor software development tools have significant weaknesses**
- **Cost**
  - **Desire for increased integration drives SoC adoption**
- **Energy efficiency**

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Why Consider Alternatives?

"As the industry shifts from second-generation, 2G, to 3G wireless we see the percentage of the physical layer MIPS that reside in the DSP dropping from essentially 100 percent in today's technology for GSM to about 10 percent for wideband code-division multiple access (WCDMA)."

Texas Instruments
IEEE Communications Magazine
January 2000

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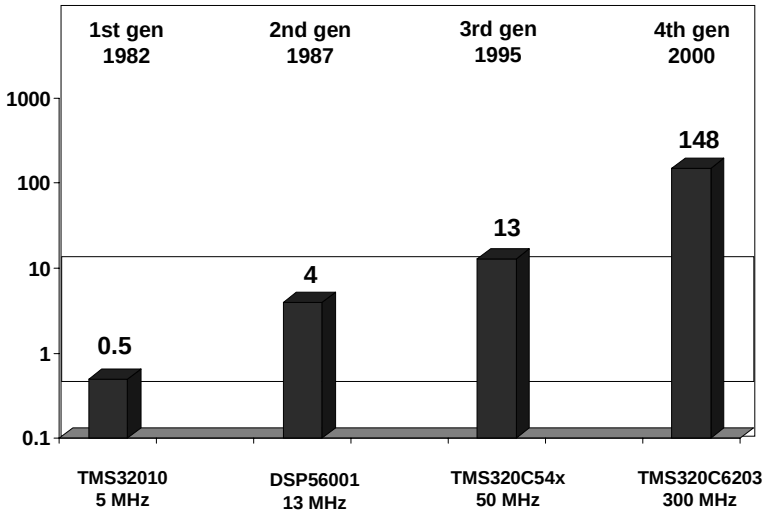
Processor DSP Speed:
BDTImarks™ (Higher is Better)



Speech

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Processor DSP Speed:
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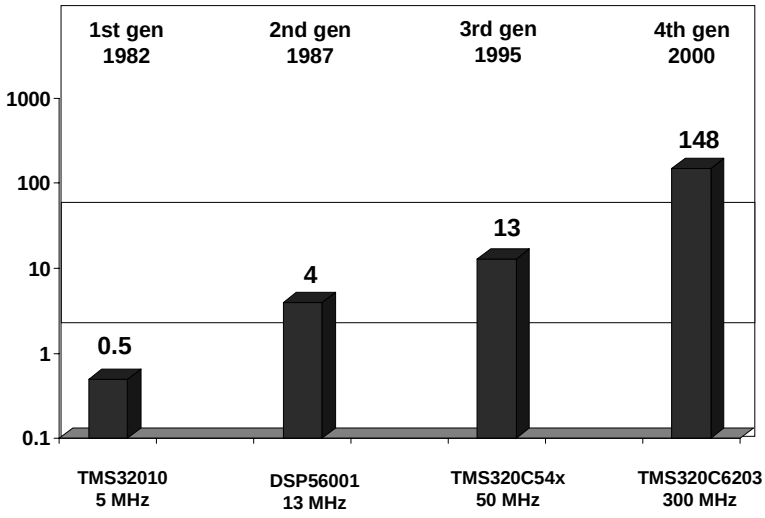

"2G" Wireless

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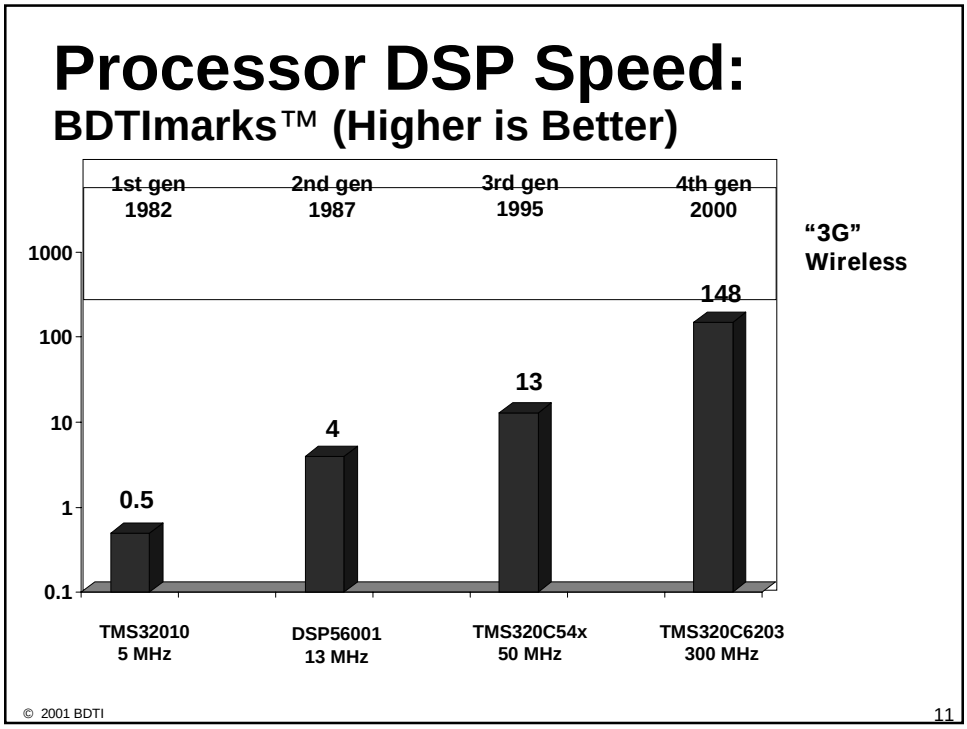

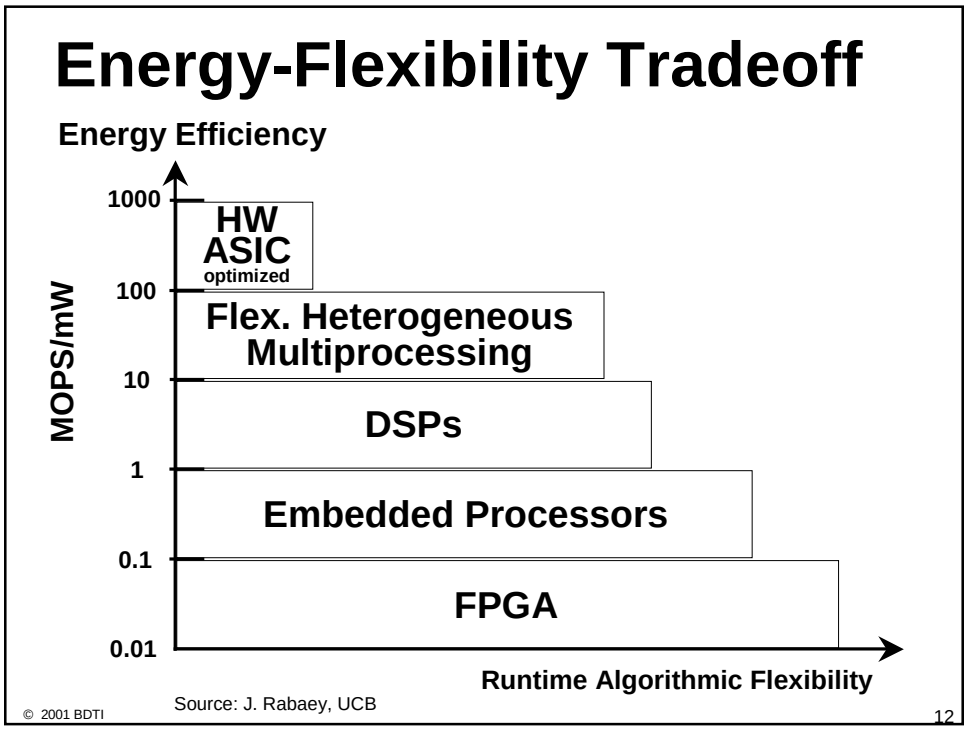

Key Alternatives

- General-purpose processors
- Massively parallel processors
- ASICs
  - DSP, CPU, coprocessor cores
  - Virtual ICs
- ASSPs
- Customizable processor cores
- Reconfigurable hardware
  - FPGAs
  - Reconfigurable processors

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GPPs and Hybrids

Today, many general-purpose processors have strong DSP capabilities

- High-performance GPPs with DSP enhancements
  - E.g., Pentium III, PowerPC 7xxx
- Embedded GPPs with and without DSP enhancements
  - E.g., SH3-DSP, LX5280
  - E.g., StrongARM

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GPPs and Hybrids

Strengths and Weaknesses

- ↑ DSP performance often strong
- ↓ Often weak on integration*
- ↑ General-purpose tools, infrastructure strong
- ↓ DSP-oriented tools, infrastructure may be weak
- ↑ Widely known, large installed base
- ↑ Compatibility (in some cases)
- ↓ Dynamic features can complicate real-time operation (mostly in high-perf. GPPs)

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ASICs

- A chip designed for a specific end product or group of end products
- Typically contains some non-programmable hardware
  - E.g., special-purpose algorithm engines
- May contain one or more processor cores
- May be a “system on chip” with memory, peripherals, special I/O, etc.
- May use a mix of custom and licensed blocks

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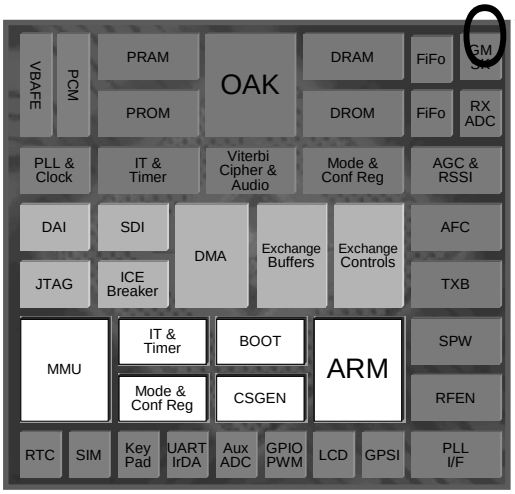
VLSI Technology's GSM SoC



Source: VLSI Technology

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ASICs

Strengths and Weaknesses

- ↑ **Offers the ultimate in tailored hardware**
  - ↑ **Speed, energy efficiency, cost/performance, …**
  - ↑ **Integration to match the product requirements**
- ↓ **Large development costs and risks vs. off-the-shelf hardware**
  - ↓ **Iteration is costly and time consuming**
- ↓ **Lengthy development cycles**
- ↓ **Hardware/software integration and whole-chip testing are particularly challenging**
- ↓ **Hardware/software partitioning typically must be done early**

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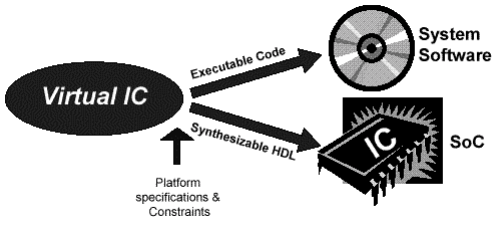
ASICs

"Virtual ICs": An Alternative Approach

An integrated behavioral model that is realizable via a variety of target architectures, platforms, and fabrication processes



Source: Ellipsis Digital Systems

Key: Behavior decoupled from implementation

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Customizable Cores

- Intended for use in SoC designs
- Certain features selectable by the chip designer (e.g., a 2nd MAC unit, cache)
- Data path can be modified
- Other features may be customizable as well
- Synthesizable HDL description generated
- Software tools automatically customized
- Examples:
  - ARC, Tensilica, Improv, Carmel2000

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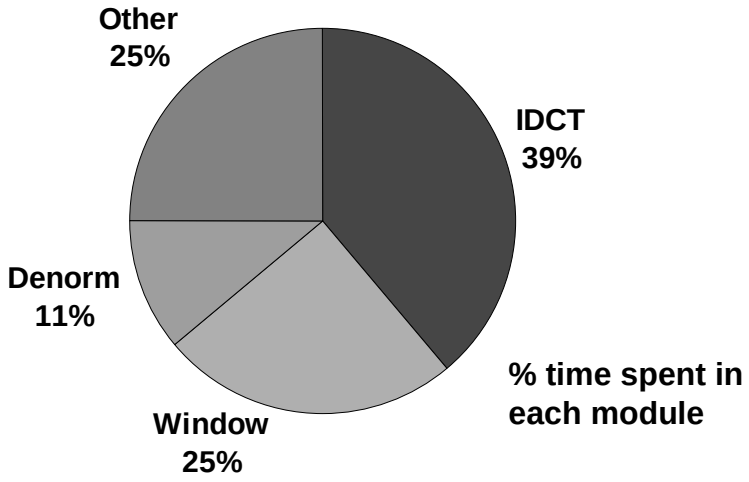
Example Application Profile: AC-3 Audio Decoder



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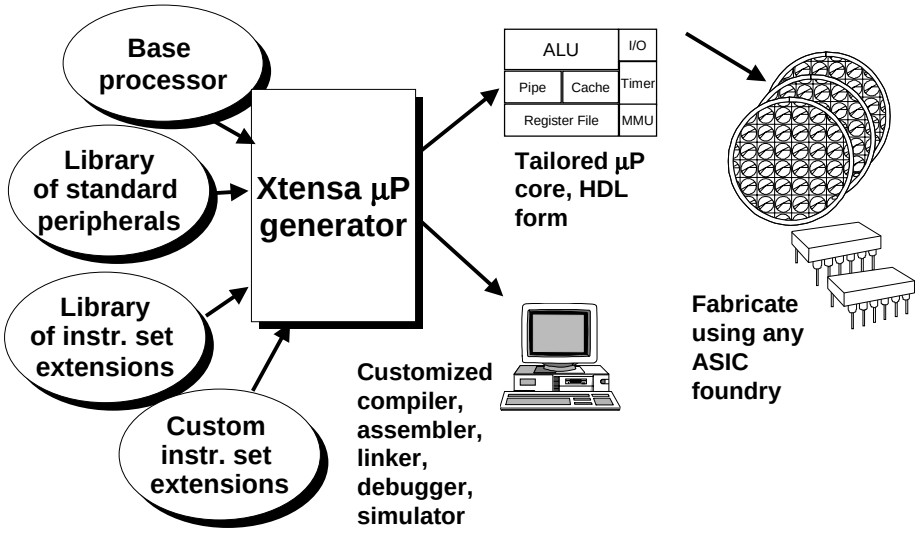
Tensilica Xtensa



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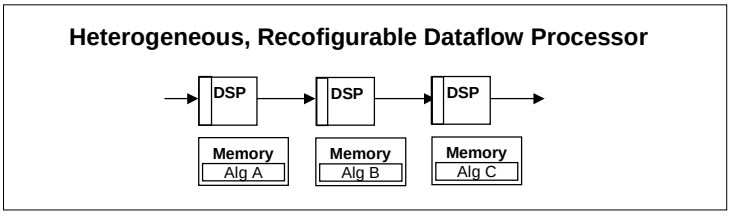
Customizable Cores
Strengths and Weaknesses

- ↑ DSP application characteristics mean that customization can yield huge gains
  - ↑ Speed, energy efficiency, cost/performance, …
- ↓ Requires a very large investment
  - ↓ *Must* design own chip
- ↓ Tools immature
  - ◆ Additional layer of complexity in tools
- ↓ Unproven technology
- ↓ Uncertain company/technology roadmaps

Reconfigurable Processors

- Blend FPGA and processor technology
- Multiple flavors:
  - Processor core + FPGA
  - Processor core w/reconfigurable data path
  - Reconfigurable, application-specific processor (or core)



Source: MorphICs Technology, Inc.

Reconfigurable Processors

Strengths and Weaknesses

- ↑ DSP application characteristics mean that customization can yield huge gains
  - ↑ Speed, energy efficiency, cost/performance, …
- ↑ Flexibility
  - Support multiple standards w/same gates
  - Support field upgrades to highly specialized hardware
- ↓ Cost, energy have been prohibitive for high-volume and portable applications
  - ↓ But application-specific approaches show promise
- ↓ Unproven
- ↓ Tools for complex DSP applications immature

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Conclusions

- Options are expanding for DSP system designers
  - New approaches
  - New products
  - New providers
- There is no single “best” choice
  - Heterogeneous SoCs increasingly common
- A key challenge: Balancing architecture-specificity with generality, flexibility
- Tools, methods, verification are key
  - Behavior, system, software, and hardware

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Resources

- **www.BDTI.com**
  - ***DSP Insider* (free email newsletter)**
  - ***Pocket Guide to DSP Processors***
  - **BDTImark2000™ DSP benchmark scores**
  - **White papers, article reprints**

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Employment Opportunities

In state-of-the-art DSP technology

- **BDTI seeks talented engineers to join our growing technical staff as DSP Engineers and DSP Analysts**
- **Outstanding location in Berkeley, California**
  - **Near San Francisco and U.C. Berkeley**
  - **Away from the crowds of Silicon Valley**
- **Excellent working environment**
  - **Interesting, varied projects**
  - **The latest DSP technology and applications**
  - **Informal, collegial atmosphere**
- **For details, please visit www.BDTI.com**

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