



C H I P S											
Vendor	BDTI Certified	Family	Floating, Fixed, or Both	Data Width	Core Clock Speed [1]	BDTImark2000™/BDTIsimMark2000™ [2]	BDTI memMark 2000™ [3]	Other Benchmark Results Available	Total On-Chip Memory, Bytes	1K Unit Price / 2Q12	Notes
Analog Devices		ADSP-218x	Fixed point	16 bits	80 MHz	240	65		8 K-104 K	\$8-31	Many family members with assorted peripherals
		ADSP-219x	Fixed point	16 bits	160 MHz	410	63		20 K-160 K	\$13-33	Enhanced version of the ADSP-218x
		ADSP-BF5xx (Blackfin)	Fixed point	16 bits	600 MHz	3360 [4,5]	72 [3,4]		52 K-328 K	\$4-43	Dual-MAC DSP with variable speed and voltage
		ADSP-BF60x (Blackfin)	Fixed point	8/16/32 bits	500 MHz	<i>6580</i>	67	OFDM	292 K-420 K	\$15-22	VLIW and SIMD architecture backward compatible with BF5xx
		ADSP-2116x (SHARC)	Both	32/40 bits	110 Mhz	<i>600</i>	34		128 K	\$26-36	SIMD architecture supporting multiprocessor topologies
		ADSP-2126x (SHARC)	Both	32/40 bits	200 MHz	1090	34		512 K-768 K	\$7-25	Features SIMD, strong multiprocessor support
		ADSP-213xx (SHARC)	Both	32/40 bits	400 MHz	2050	34		384 K-1024 K	\$10-43	SHARC with a lengthened pipeline for higher clock speeds
		ADSP-214x (SHARC)	Both	32/40 bits	450 MHz	<i>n/a</i>	<i>n/a</i>		256K-1152K	\$8-37	Hardware-based filter accelerators, audio-focused peripherals
	ADSP-TS20x (TigerSHARC)	Both	8/16/32/40 bits	600 MHz	6400 [5]	52 [5]		512 K-3 M	\$184-339	4-way VLIW with SIMD capabilities; uses eDRAM	
Freescale		B4860 (SC3900)	Fixed point	16 bits	1.2 GHz	<i>37460 [4]</i>	52		9856 K	\$164-295	Six SC3900 DSP cores, targets base station applications
		DSP563xx/5672x	Fixed point	24 bits	275 MHz	820 [4]	50		<i>n/a</i>	\$6-46	Many audio-oriented parts; binary-compatible with '560xx
		DSP56F8xx (56800)	Fixed point	16 bits	80 MHz [6]	110	78		28 K-152 K	<i>n/a</i>	Contains many microcontroller-like features
		DSP5685x/56F8xxx (56800E)	Fixed point	16 bits	120 MHz	<i>340</i>	79		14 K-612 K	<i>n/a</i>	Enhanced version of the '568xx
		MSC71xx (SC1400 core)	Fixed point	16 bits	300 MHz	<i>3370</i>	67		408 K-472 K	\$37-43	Based on SC1400 licensable core
		MSC81xx (SC140 core)	Fixed point	16 bits	500 MHz	5610 [4]	67 [4]		1440 K	\$78-121	Based on SC140-compatible core; most chips use four cores
		MSC814x (SC3400 core)	Fixed point	16 bits	1 GHz	11900 [4]	67 [4]	OFDM	10.9 M	\$122-147	Based on SC3400 core; quad-core chip
	MSC815x/825x (SC3850 core)	Fixed point	16 bits	1 GHz	15420 [4]	67 [4]		1728 K-4608 K	\$68-157	Based on SC3850 core; devices with 4 and 6 cores available	
Microchip		dsPIC3xF	Fixed point	16 bits	70 MHz	<i>190</i>	78		6 K-588 K	\$2-8	Hybrid microcontroller/DSP
NXP		TriMedia 3270 core	Both	8/16/32 bits	350 MHz	<i>n/a</i>	<i>n/a</i>	Video Encoder/Decoder	16 M	<i>n/a</i>	VLIW media processor with SIMD capabilities
PicoChip		PC102	Fixed point	16 bits	160 MHz	<i>n/a</i>	<i>n/a</i>	OFDM	1 M	\$99	Massively parallel chip with 344 processors
Qualcomm		Qualcomm Hexagon V2 (1 thread) ⁷	Fixed point	16 bits	100 MHz (per thread)	<i>1550</i>	53		<i>na</i>	<i>na</i>	Multi-threaded device (6 threads, each running at 100 MHz) Projected best-case BDTIsimMark2000 for 6 threads is 9300
		Qualcomm Hexagon V4 (1 thread) ⁷	Fixed point	16 bits	233 MHz (per thread)	<i>4220</i>	57		<i>na</i>	<i>na</i>	Multi-threaded device (3 threads, each running at 233 MHz) Projected best-case BDTIsimMark2000 for 3 threads is 12660
		Qualcomm Hexagon V5 (1 thread) ⁷	Fixed point	8/16/32 bits	267 MHz (per thread)	<i>4840</i>	57		<i>na</i>	<i>na</i>	Multi-threaded device (3 threads, each running at 267 MHz) Projected best-case BDTIsimMark2000 for 3 threads is 14520
		Qualcomm Hexagon V5 (1 thread) ⁷	Floating point	8/16/32 bits	267 MHz (per thread)	<i>2400</i>	43		<i>na</i>	<i>na</i>	Multi-threaded device (3 threads, each running at 267 MHz) Projected best-case BDTIsimMark2000 for 3 threads is 7200
Texas Instruments		OMAP35x	Fixed point	8/16/32 bits	720 MHz	<i>5450</i>	78		320 K	\$23-38	Metrics for ARM Cortex-A8 core only (optional 'C64x+ DSP available)
		TMS320 [C/F] 280x/281x/282x	Fixed point	32 bits	150 MHz	<i>n/a</i>	<i>n/a</i>		40 K-582 K	\$3-16	Hybrid microcontroller/DSP; assembly-compatible w/ 'C24x
		TMS320F2802x/2803x/2806x	Fixed point	32 bits	90 MHz	<i>n/a</i>	<i>n/a</i>		40 K-422 K	\$1-8	Peripherals and accelerators targeting control applications
		TMS320C54x	Fixed point	16 bits	160 MHz	500 [4]	64 [4]		24 K-336 K	\$4-134	Many specialized instructions
		TMS320C55x	Fixed point	16 bits	300 MHz	1460	75		64 K-376 K	\$2-17	Dual-issue, dual-MAC DSP; assembly-compatible w/ 'C54x
		TMS320C64x	Fixed point	8/16 bits	1 GHz	9130	54	OFDM	160 K-1056 K	\$18-202	Adds quad-MAC capabilities and specialized operations to 'C62x
		TMS320DM6446	Fixed point	8/16 bits	600 MHz	6590	60	H.264 Sol. Benchmark	232 K	\$36	ARM9, C64x+ and video accelerator (BDTImark2000 for C64x+ only)
		TMS320C64x+	Fixed point	8/16 bits	1.2 GHz	13170	60	OFDM	128 K-3 M	\$10-216	Adds 8-MAC capabilities and specialized operations to 'C64x
		TMS320C66x	Fixed point	16 bits	1.5 GHz	20030 [4]	62 [4]		2M-8M	\$34-399	High performance fixed- and floating-point DSP core
		TMS320C2834x/F2833x	Floating point	32 bits	300 MHz	<i>n/a</i>	<i>n/a</i>		182 K-582 K	\$9-16	Adds floating-point unit to 'C28x
		TMS320C66x	Floating point	32 bits	1.5 GHz	12860 [4]	42 [4]		2M-8M	\$34-399	High performance fixed- and floating-point DSP core
	TMS320C67x	Floating point	32 bits	300 MHz	1500	35		72 K-264 K	\$14-33	Floating-point version of 'C62x	
	TMS320C67x+	Floating point	32 bits	300 MHz	<i>n/a</i>	<i>n/a</i>		480 K-672 K	\$7-29	Adds registers and audio-oriented instructions to the 'C67x	
Tilera		TILE64	Fixed point	8/16 bits	866 MHz	<i>n/a</i>	<i>n/a</i>	OFDM	5120 K	\$896	64 core chip, 3-way VLIW with SIMD capabilities

NOTES:

[1] Clock speed is for fastest family member.

[2] The BDTImark2000 and BDTIsimMark2000 provide summary measures of DSP speed, based on scores on the BDTI DSP Kernel Benchmarks™. **Higher is faster.** Both scores are calculated with the same formula, but BDTIsimMark2000 scores may use projected clock speeds. BDTImark2000 scores are shown in **bold** and BDTIsimMark2000 scores in *italic*. See www.BDTI.com/Resources/BenchmarkResults for more information and scores.

[3] The BDTImemMark provides a summary measure of memory use in signal processing applications; higher is better.

[4] Score for one core. Some family members contain multiple cores. Details available from BDTI.

[5] Score does not apply to some family members, which use slightly different architectures. Details available from BDTI.

[6] The DSP56F8xx requires two clock cycles per instruction cycle.

[7] Multi-threaded device. BDTIsimMark2000 result listed is the score for a single thread. The 'Notes' column lists the projected best case score using the maximum number of available threads (not an official BDTIsimMark2000 score).

This processor has BDTI Certified benchmark results available.

CORES											
Licensors		Family	Floating, Fixed, or Both	Data Width	Core Clock Speed [1,2]	BDTI _{mark} 2000™ / BDTI _{sim} Mark2000™ [3]	BDTI memMark 2000™ [4]	Other Benchmark Results Available [5]	Total Core Memory Space, Bytes	Die Area [2]	Notes
ARC		ARC 600/ARC XY	Fixed point	16/32 bits [6]	180 MHz [7]	n/a	n/a		4 G	0.77 mm ² [7]	Customizable core with optional DSP features
		ARC 700/ARC XY	Fixed point	16/32 bits [6]	265 MHz [7]	n/a	n/a		4 G	1.1 mm ² [7]	Longer pipeline enables higher clock rate
ARM		AV 401V	Fixed point	16/32 bits	n/a [8]	n/a	n/a	H.264 Sol. Benchmark	4 G	n/a [8]	Licensable video subsystem based on ARC 700 plus accelerators
		ARM7	Fixed point	32 bits	145 MHz	160	57		4 G	0.28 mm ²	Widely licensed 32-bit microprocessor core
		ARM9	Fixed point	32 bits	255 MHz	320	74		4 G	n/a	Adds separate bus for data access, deeper pipeline to ARM7
		ARM9E	Fixed point	16/32 bits	265 MHz	550	72		4 G	1.7 mm ²	ARM9 enhanced with single-cycle MAC unit
		ARM1136	Fixed point	16/32 bits	330 MHz	1160	72		4 G	2.3 mm ²	Adds SIMD, load/store unit, branch prediction, deeper pipeline
		ARM1176	Fixed-point	16/32 bits	335 MHz	1200	72	Video Encoder/Decoder	4 G	2.5 mm ²	Very similar to ARM1136
		Cortex-A8	Fixed point	8/16/32 bits	n/a [8]	7.6 per MHz	78	Video Encoder/Decoder	4 G	n/a [8]	Dual-issue superscalar architecture with NEON DSP extensions
CEVA		Cortex-R4	Fixed point	16/32 bits	n/a [8]	3.8 per MHz	73		4 G	n/a [8]	Dual-issue superscalar architecture; software compatible with ARM9E
		CEVA-TeakLite	Fixed point	16 bits	170 MHz	n/a	n/a		256 K	0.4 mm ²	Single-MAC, single-issue DSP core
		CEVA-TeakLite II	Fixed point	16 bits	200 MHz	n/a	n/a		4 M	0.5 mm ²	Faster version of CEVA-TeakLite
		CEVA-TeakLite III	Fixed point	16/32 bits	335 MHz	2140	69		4 G	1.14 mm ²	Dual-MAC DSP core; backward compatible with TeakLite II
		CEVA-Teak	Fixed point	16 bits	150 MHz	n/a	n/a		8 M	0.9 mm ²	Dual-MAC DSP core
		CEVA-X1620	Fixed point	8/16 bits	330 MHz	2660	67		4 G	2.6 mm ²	8-way VLIW, dual-MAC DSP core
Coreworks		CEVA-X1641	Fixed point	8/16 bit	600 MHz	n/a	n/a		4 G	n/a	8-way VLIW, quad-MAC DSP core supporting SIMD operations
ITRI		Sideworks CWcomp4465	Fixed point	16 bits	209 MHz	2440	48		4G	0.68 mm ²	Customized SideWorks DSP engine + FireWorks 32-bit RISC CPU
MIPS		PAC DSP	Fixed point	8/16/32 bits	n/a [8]	8.8 per MHz	43		4G	n/a [8]	4-way VLIW, quad-MAC DSP core
Tensilica		MIPS32 24KE (with DSP ASE)	Fixed point	16/32 bits	335 MHz	1000	73		4 G	2.0 mm ²	MIPS core with SIMD DSP extensions
Toshiba		ConnX 545CK	Fixed point	18 bits	245 MHz	4070	69		4 G	5.49 mm ²	VLIW-based customizable core; with optional DSP features
VeriSilicon		Venezia (MeP + IVC2)	Fixed point	8/16/32 bits	n/a [8]	7.9 per MHz	69		4G	n/a [8]	MeP core: 32-bit RISC; IVC2 coprocessor: 64-bit SIMD
		ZSP _{neo}	Fixed point	16/32 bits	165 MHz	n/a	n/a		256 K	0.45 mm ²	Single-MAC, scalar variant of the ZSP400
		ZSP200	Fixed point	16/32 bits	165 MHz	n/a	n/a		256 K	0.7 mm ²	Single-MAC, 2-way superscalar variant of the ZSP400
		ZSP400	Fixed point	16/32 bits	165 MHz	780	74		256 K	1.3 mm ²	Dual-MAC, 4-way superscalar DSP core
		ZSP410	Fixed point	16/32 bits	185 MHz	870	74		4 G	1.4 mm ²	Enhanced ZSP400 with instruction cache
		ZSP500	Fixed point	16/32 bits	205 MHz	1620	68		64 M	2.2 mm ²	Second-generation ZSP; dual-MAC, 4-way superscalar
		ZSP540	Fixed point	16/32 bits	200 MHz	n/a	n/a		64 M	2.7 mm ²	Quad-MAC, 4-way variant of the ZSP500
	ZSP600	Fixed point	16/32 bits	175 MHz	n/a	n/a		64 M	3.1 mm ²	Quad-MAC, 6-way variant of the ZSP500	

FPGAs						
Vendor		Family	Core Clock Speed	BDTI Benchmark Score Available	1K Unit Price 2Q2011	Notes
Altera		Stratix II EP2S15F672C5	Slow speed grade	OFDM	\$38	FPGA with hardwired DSP features, such as multipliers
Xilinx		Virtex-4 SX25-10FF668C	Slow speed grade	OFDM	\$89	FPGA with hardwired DSP features, such as multipliers
		Virtex-4 XC4VFX140-11FF1760C4006	Med. speed grade	OFDM	\$1,280	FPGA with hardwired DSP features, such as multipliers

Notes:
 [1] Worst-case clock speed.
 [2] All core data is for the TSMC CL013G process and ARM Artisan SAGE-X library (devices with the "BDTI Certified" box checked conform to BDTI's standardized conditions for processor cores).
 [3] The BDTI_{mark}2000 and BDTI_{sim}Mark2000 provide summary measures of DSP speed, based on scores on the BDTI DSP Kernel Benchmarks(tm). **Higher is faster.** Both scores are calculated with the same formula, but BDTI_{sim}Mark2000 scores may use projected clock speeds. BDTI_{mark}2000 scores are shown in **bold** and BDTI_{sim}Mark2000 scores in *italic*. See www.BDTI.com/Resources/BenchmarkResults for more information and scores.

[4] The BDTI_{mem}Mark provides a summary measure of memory use in signal processing applications; higher is better.
 [5] Additional BDTI Benchmark results available at www.BDTI.Com
 [6] Native multiplier width(s). Users may add custom instructions that support other data widths.
 [7] Assumes use of optional DSP extensions but no other optional features.
 [8] BDTI does not have clock speed and silicon area for this processor based on BDTI's standardized conditions for processor cores.

This processor has BDTI Certified benchmark results available.