Optimized DSP Software • Independent DSP Analysis

Enabling Technologies for SDR: Comparing FPGA and DSP Performance

Berkeley Design Technology, Inc.
2107 Dwight Way, Second Floor
Berkeley, California 94704
USA
+1 (510) 665-1600

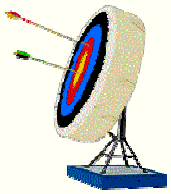
info@BDTI.com
http://www.BDTI.com

Presentation Goals

Challenges in Performance Comparison:
- Comparing DSP processor and FPGA performance
- Comparing performance between different FPGAs
- A benchmark for communications applications

Present Results from BDTI's *FPGAs for DSP* 2006 Report:
- Benchmark results for Freescale and TI DSPs
- Benchmark results for DSP-oriented FPGAs from Altera and Xilinx

Conclusions



Performance Analysis

- Evaluating the performance of FPGAs for DSP applications is tricky
- Common MMACS metric is oversimplified to the point of absurdity
  - FPGAs vendors use distributed-arithmetic benchmark implementations that require fixed coefficients
  - MMACS metric overlooks need to dedicate resources to non-MAC tasks
  - Many important DSP algorithms don't use MACs at all!

Alternative Approach: Application Benchmarks

Use a full application, e.g., N channels of an OFDM receiver

Hazards:

- Applications tend to be ill-defined
- Hand-optimization usually required in real-world applications
  - Costly, time-consuming to implement
  - Evaluates programmer as much as processor
  - What is a "reasonable" benchmark implementation?

Solution: Simplified Application Benchmark

BDTI's benchmark is based on a simplified OFDM receiver

- Closely resembles a real-world application
- Simplified to enable optimized implementations
- Constrained to ensure consistent, reasonable implementation practices

Benchmark goals: (two choices)

- Maximize the number of channels
- Minimize the cost per channel

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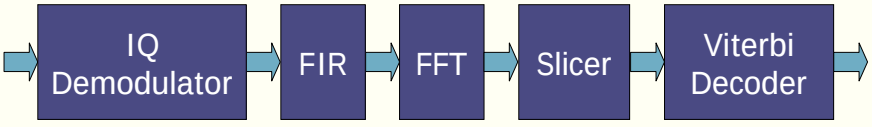
Benchmark Overview

Flexibility is an asset:

- Algorithms range from table look-ups to MAC-intensive transforms
- Data sizes range from 4 to 16 bits
- Data rates range from 40 to 320 MB/s
- Data includes real and complex values



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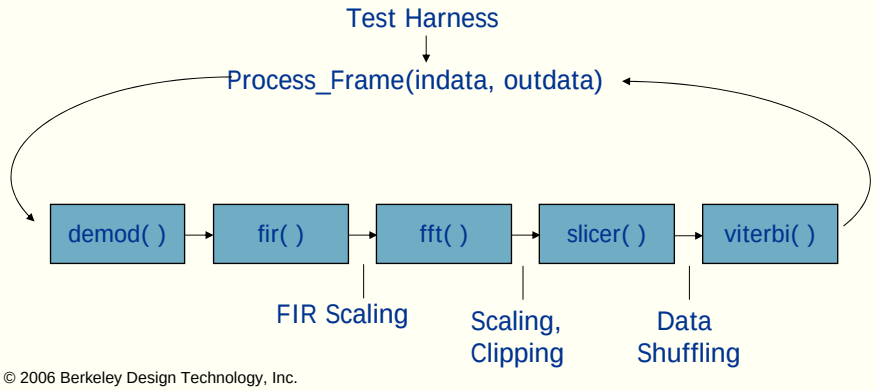
DSP Processor Implementations

DSPs execute the benchmark functions sequentially

Data is processed in frames of 256 samples

DSP processor clock speeds of 400 MHz & 1 GHz

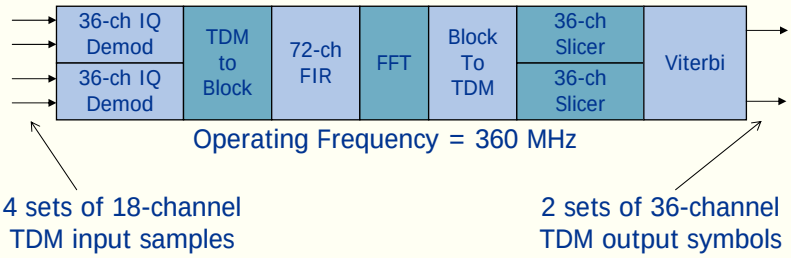


FPGA Implementations

FPGAs exploit three-levels of parallelism:

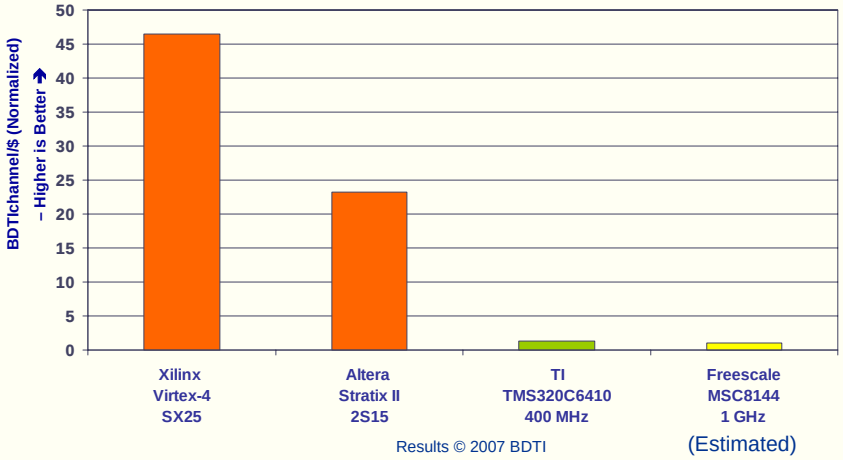
- Within each receiver block, multiple operations are executed concurrently
- All receiver blocks operate concurrently
- Multiple receiver modules are used on the same chip

Simplified diagram of a single receiver module in a Xilinx Virtex-4 implementation:



BDTI Communications Benchmark (OFDM)™

New BDTI-Certified Cost-Performance Optimized Results



Results © 2007 BDTI

Why Use a DSP?

- Many applications are not amenable to efficient FPGA implementations
  - Parallelism is sometimes inherently limited
  - Ultimate speed is not always the first priority
- Many skilled engineers with DSP processor expertise
- Still easier to use
  - More familiar paradigm
  - Lots of in-house and third-party IP
  - Strong tools

Conclusions

High-end FPGAs can outstrip DSPs on certain DSP tasks
- Computation-intensive, highly parallelizable tasks

High-end FPGAs can beat DSPs in terms of performance per dollar on these tasks

DSP have the advantage in development infrastructure, time-to-market, developer familiarity

In many applications, a heterogeneous combination of computing engines is desirable
- Expect to see more heterogeneous processor chips

The "best" architecture depends on the details of the application

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Future Work

- Power benchmarking for FPGAs
  - Milliwatts per channel?
  - FPGAs versus DSP processors
  - FPGAs versus FPGAs
- Benchmarking high-level design tools
  - Performance, ease of use, and productivity
  - C to FPGA
  - Simulink to FPGA
- Processors on FPGAs
  - Performance, tools, hardware-software co-design
  - Altera Nios II
  - Xilinx MicroBlaze

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For More Information...

www.BDTI.com

Inside [DSP] newsletter and website

Benchmark scores for dozens of processors

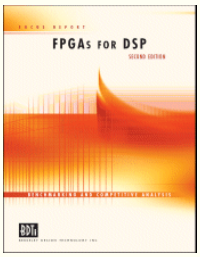
Pocket Guide to Processors for DSP

- Basic stats on over 40 processors

Articles, white papers, and presentation slides

- Processor architectures and performance
- Signal processing applications
- Signal processing software optimization

comp.dsp FAQ



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