Optimized DSP Software • Independent DSP Analysis

Selecting Application Processors for Mobile Multimedia

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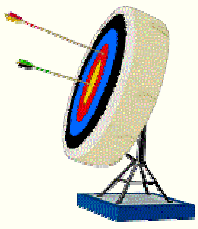
Presentation Goals

Provide an introduction to and independent perspective on:

- Key selection criteria and trends for application processors
- Common approaches to multimedia acceleration used in application processors
- Key strengths and weaknesses of each approach
- Key strengths and weaknesses of representative processors from each category



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Application Processors Defined

Run "user applications" in smart phones, PDAs, etc.
Support complex OSs
- Symbian, Windows CE, PalmOS, or Linux

Emphasize multimedia processing
- Audio, video, still image, and 2D and 3D graphics
- Media player, camera, games

Support Java for games and other downloaded apps
Support security features for m-commerce, DRM, etc.
Do not handle "baseband" (wireless communications)

This presentation focuses on audio and video tasks

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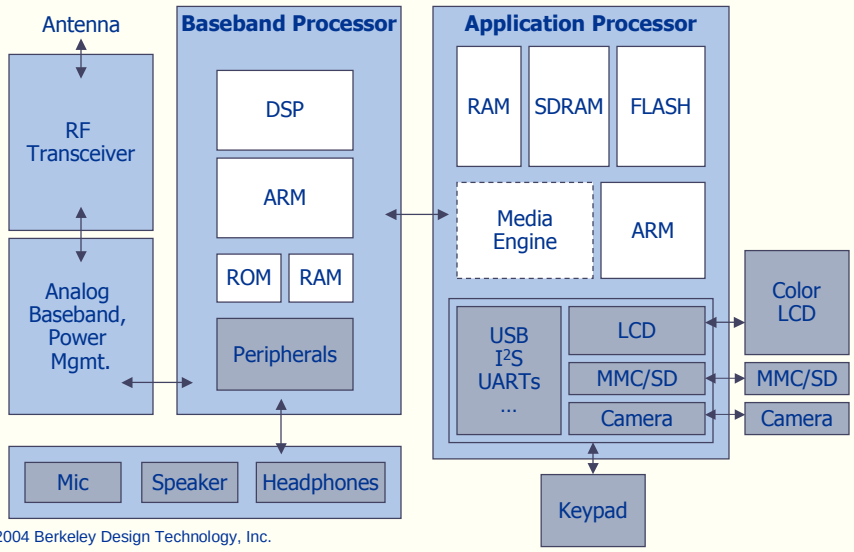
Application vs. Baseband



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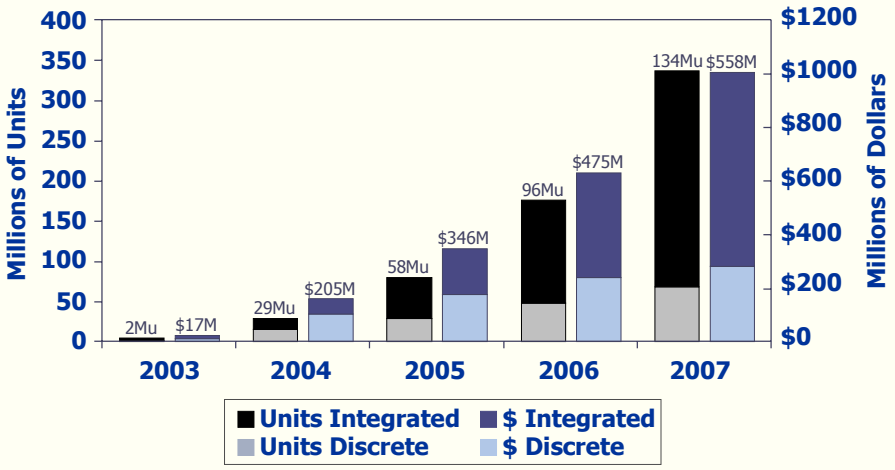
Application Processor Market

Application Processor Sales Forecast



Source: Forward Concepts

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Motivations for Mobile Multimedia

Add features to differentiate in a crowded market

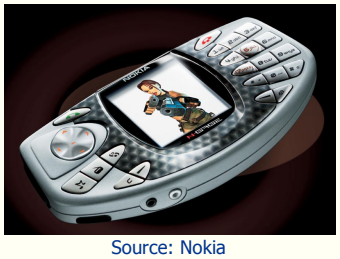
- Examples: camera or music player in phone or PDA

Integrate features of separate products for convenience

- Examples: PDA + phone, game machine + phone

For service providers:

- Drive growth in mature markets
- Increase service revenues
- Differentiate via features



Source: Nokia

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Application Processor Needs

Key Considerations

Speed
- Multimedia tasks
- Multitasking

System cost and size
- Chip cost
- Memory use
- Memory integration
- Peripheral integration
  - Interfaces for LCD, camera, keypad, flash, baseband processor, many others

Energy efficiency

Flexibility, expandability
- Performance headroom
- Open software environment
  - Operating systems
  - Java

Application development
- Compatibility
- Roadmap
- Multi-vendor support
- Tools and support
- Installed base
- Off-the-shelf software
- Reference designs
- Services

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Processor Vendors

Vendor	Notes
ARM	Family of GPP cores used in most application processors
Emblaze	ER45xx family of application processors and video coprocessors
Intel	PXA family of application, application/baseband processors
MIPS	Family of GPP cores used in some application processors
Motorola	Several families of application, application/baseband processors
NeoMagic	MiMagic family of application processors
Qualcomm	MSM7xxx family of application/baseband processors
Renesas	Family of SH-based application processors
Samsung	S3Cxxxx family of application processors
STMicro	MIPI-compliant Nomadik application processors
TI	OMAP families of application, application/baseband processors

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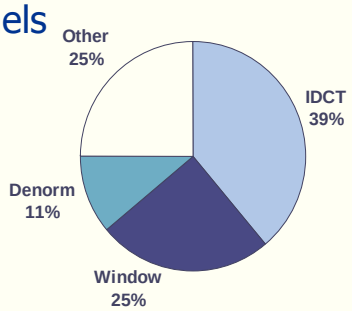
Algorithm Kernel Benchmarks

The BDTI Benchmarks™ are based on signal-processing algorithm kernels

- DSP algorithm kernels are the most computationally intensive portions of DSP applications



Example algorithm kernels include FFTs, IIR filters, and Viterbi decoders

Application-relevant algorithm kernels are strong predictors of overall performance

Kernels require only modest programming effort

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Kernel Benchmark Weaknesses

Algorithm kernel benchmarks are good for measuring general signal-processing performance, but they…

- Do not measure system-level performance
- Do not measure OS overhead
- Require careful application for multi-core processors
- Cannot be easily applied to hardware accelerators, FPGAs, etc.

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Task Benchmarks

Model a key signal-processing task
- E.g., MPEG-4 video decode
- ↑ Easier to implement than a full application
- ↑ Fairly representative of actual workload
- ↓ Do not capture effects of combining multiple tasks
- ↓ Less general than a set of kernel benchmarks

Can be structured as a "pin-to-pin" benchmark
- ↑ Allows comparison of different types of architectures
- ↑ Simplifies programming rules
- Benchmarks the entire system
  - Capture effects of memory size, bandwidth, etc.

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Full-Application Benchmarks

- ↑ Potential for highly accurate results
  - ↓ Results useful only for specific application (or highly similar applications)
  - ↓ Applications tend to be ill-defined
- Benchmarks the entire system
- ↓ Costly and time-consuming to implement
  - ↓ Measures programmer as much as processor
  - What is a "reasonable" benchmark implementation?
- ↓ For processors, similar results via simpler approaches
  - But this is not true for all implementation technologies

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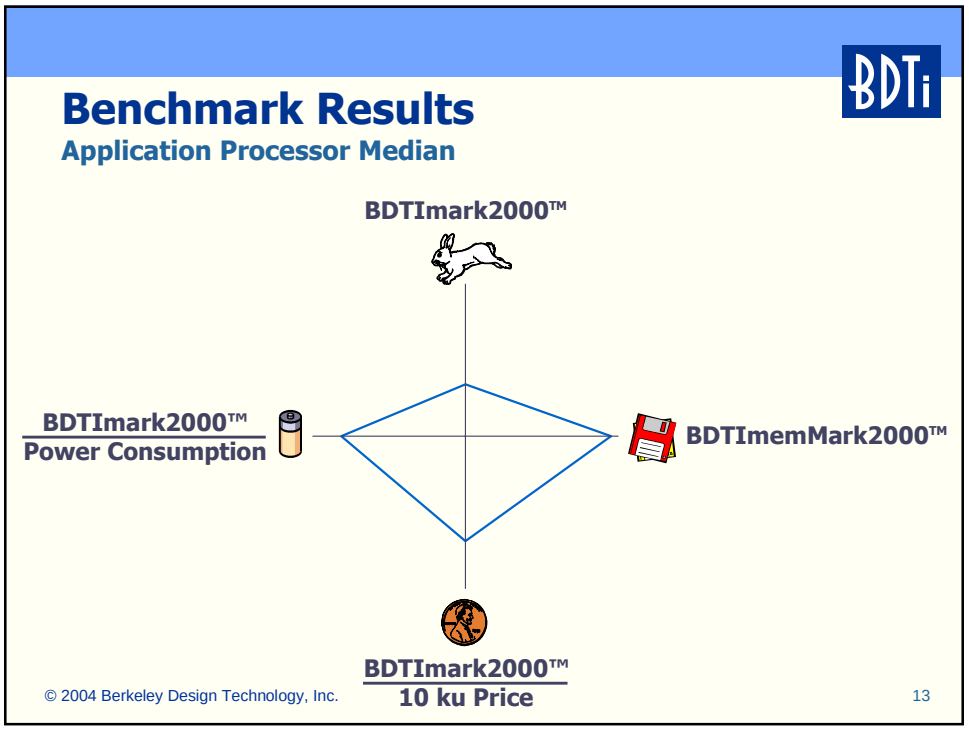

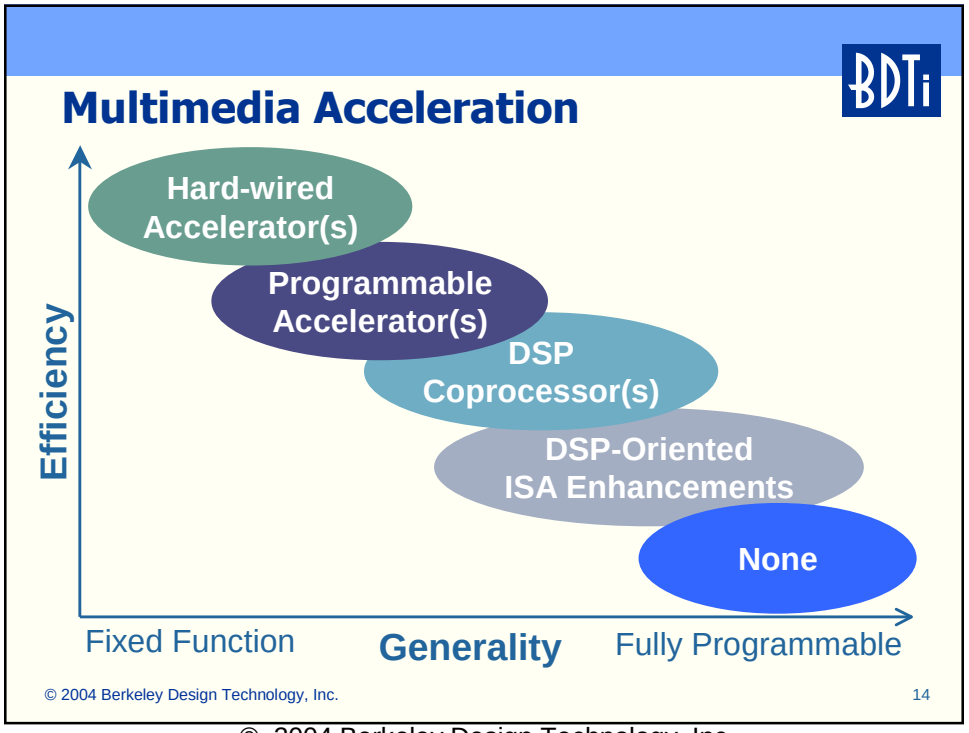

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No Multimedia Acceleration

Strengths and Weaknesses

- ↓Rely on high clock speeds to attain performance
- ↓Memory architecture is frequently a weak link
- ↑Simple programming model
- ↓Dynamic features complicate programming
  - ↓Complicate optimization and ensuring real-time performance
- ↑Good tools, some with DSP support
- ↑Mature architectures, stable roadmaps
- ↑Very good third-party software support
- ↑Very good compatibility

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Samsung S3C24xx

Based on ARM9 core
- No DSP-specific features
- Multiplier has data-dependent throughput

32 Kbytes of cache, but no SRAM

S3C2410 multi-chip package integrates 32 MB SDRAM, 32 MB flash

S3C2410 shipping at 266 MHz, 2.0 V
- Pricing starts at $11 (10 ku) for 203 MHz version

S3C2440 sampling at 533 MHz, 1.3 V
- Pricing starts at $19 (10 ku) for 400 MHz version

MPEG-4 decode (simple profile, level 1, QCIF, 15 fps): 10-20 MHz (BDTI estimate)

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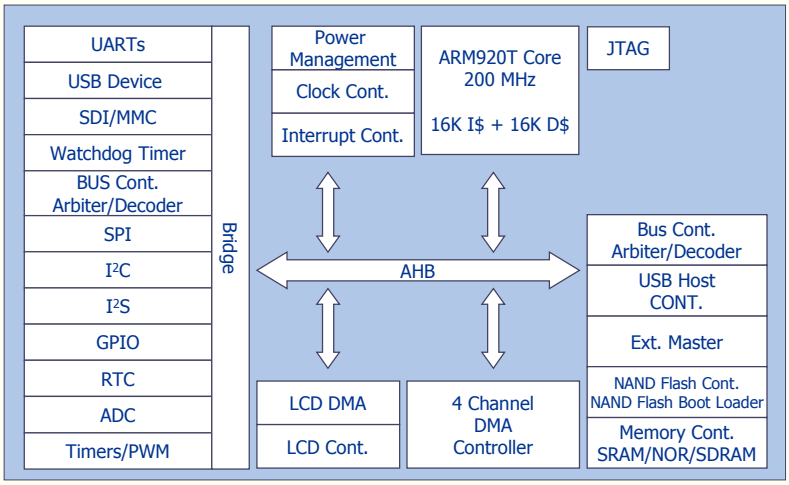
S3C2410 On-Chip Integration



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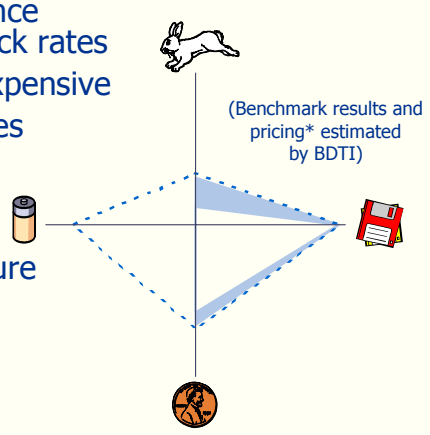
Samsung S3C24xx

Strengths and Weaknesses

- Moderate DSP speed and cost-efficiency
  - ↓ No DSP features; performance comes mainly from high clock rates
- ↑ Some family members are inexpensive
- ↓ All on-chip memories are caches
  - ↑ Large stacked SRAM and flash memories on some family members
- ↑ Simple, uniprocessor architecture
- ↑ Extensive compiler, OS, and third-party support
- ↑ Excellent compatibility

*Based on initial pricing provided by Samsung



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DSP-Oriented ISA Enhancements

Strengths and Weaknesses

- Modest enhancements, e.g., single-cycle multiply-accumulates on ARM9E
- Extensive enhancements, e.g., 8-way SIMD on PXA27x
- Strengths and weaknesses resemble those of non-enhanced GPPs, but…
  - ↑ Speed and efficiency are typically better
  - ↑ Memory architecture is sometimes better
  - ↓ Programming model may be more complex
  - ↓ ISA enhancements reduce compatibility

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Intel PXA255/26x (XScale Based)

XScale implements ARMv5TE instruction set, but adds:
- SIMD dual-16-bit MAC
- 40-bit accumulator

XScale microarchitecture differs from ARM cores
- Longer pipeline: 7 stages vs. 5 stages
- Adds branch prediction

PXA255/26x include 66 Kbytes of cache, but no SRAM

PXA26x "stacked" with up to 32 Mbytes of flash

Speed/voltage scaling: 400 MHz/1.3 V to 200 MHz/1.0 V

Shipping at 400 MHz, $35 (10 ku)

MPEG-4 decode (simple profile, level 1, QCIF, 15 fps): 10-20 MHz (BDTI estimate)

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Intel PXA27x

XScale with Wireless MMX extensions

Wireless MMX further extends the architecture

- Superset of integer instructions from x86 MMX and SSE instruction sets
- Eight 8-bit, four 16-bit, two 32-bit, or one 64-bit operation with a single instruction.
- Sixteen new 64-bit registers

PXA27x includes 66 Kbytes of cache and 256 Kbytes of level-two SRAM

Most PXA27x family members offer "stacked" memory

- Example: PXA271 offers 32 Mbytes of flash and 32 Mbytes of SDRAM

Speed/voltage scaling: 624 MHz/1.55 V–104 MHz/0.9 V

Shipping at 312 MHz, $32 (10 ku)

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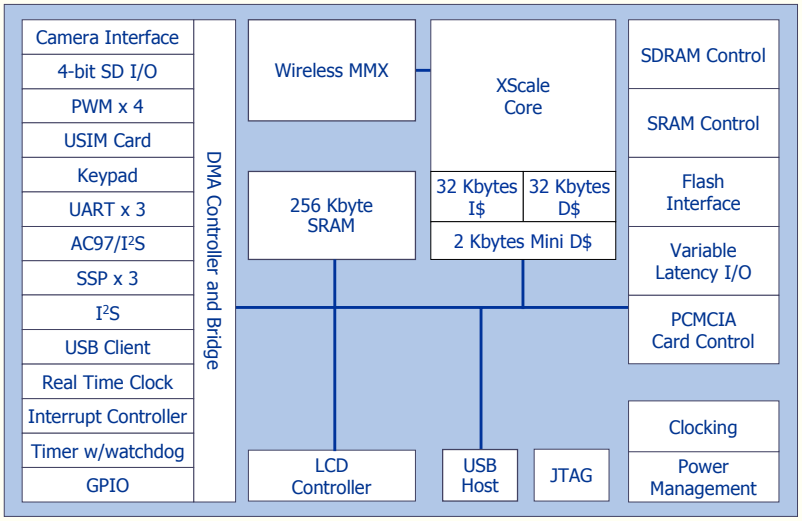
PXA27x On-Chip Integration



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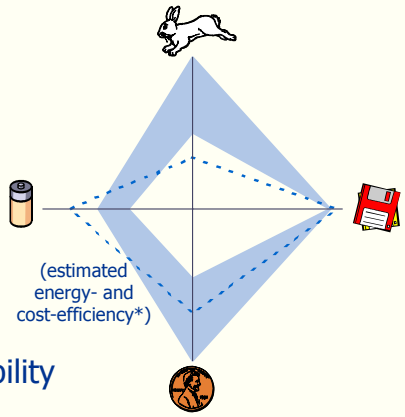
Intel PXA27x

Strengths and Weaknesses

- ↑ Very fast
- ↓ Very expensive
  - ↑ Some family members are highly cost-efficient
  - ↑ Large stacked flash memories on most family members may offset cost
- • Moderate energy-efficiency
  - ↑ Unusual speed/energy flexibility
- ↑ Good OS and compiler support
- ↑ Large on-chip memory system



*Based on initial power and pricing data provided by Intel

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DSP Coprocessor(s)

Strengths and Weaknesses

- ↑ Enough speed for most tasks
  - ↓ But insufficient for cutting-edge tasks
- ↑ Architecture designed for signal-processing
  - ↑ Eases optimization, ensuring real-time behavior
  - ↑ Improved energy efficiency
- ↑ Improved task-switching efficiency, responsiveness
- ↓ Complex (multiprocessor) programming model
- ↑ Generally good tools with signal-processing features
- ↑ Good third-party software component support
- ↑ Good compatibility for some
- ↑ Some mature architectures, stable roadmaps

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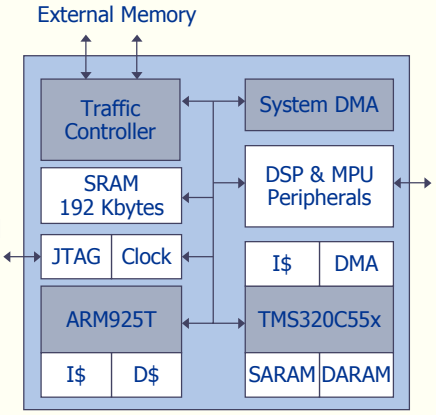
Texas Instruments OMAP5910

- 150 MHz ARM9 core
  - 32-bit multiplier with data-dependent throughput
- 150 MHz 'C55x core
  - Up to two 16-bit MACs per cycle
  - Accelerators for video, imaging
- Cores interact via mailbox registers, shared memory, and DMA transfers
- 320 Kbytes of on-chip cache and SRAM
- Extensive development support, including GPP-DSP API, multi-core-aware tools
- Excellent 3rd-party software support
- Claim: MPEG-4 decode (simple profile, level 1, QCIF, 15 fps): 10-15 MHz
- Shipping at $22 (10 ku)



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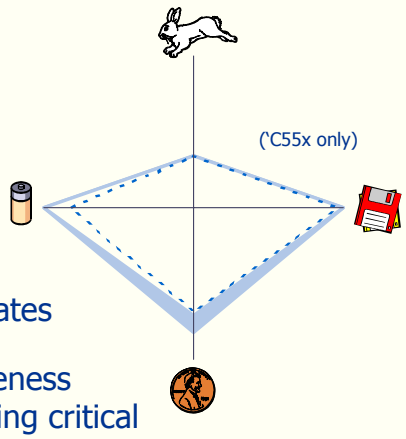
Texas Instruments OMAP5910

Strengths and Weaknesses

- ↑ Good energy-, memory-, and cost-efficiency
  - ↑ Image, video accelerators boost performance
- ↑ Memory system designed for signal processing
- ↑ Both cores well established
  - ↑ Strong tools, third-party software support
  - ↑ Design-house network
- ↓ Dual-core architecture complicates programming
  - ↑ But may improve responsiveness
  - Careful application partitioning critical



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Programmable Accelerator(s)

Strengths and Weaknesses

- ↑ Architecture designed for media processing
  - ↑ Potential for strong performance
  - ↑ Potential for good energy efficiency
  - ↓ May rely on GPP core for media "glue logic"
- ↓ Complex, unique, unfamiliar programming models
- ↓ Tools generally immature
- ↓ Very limited third-party software support
- ↓ Flexibility may be limited by architecture or by programming complexity
- ↓ Little compatibility

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NeoMagic MiMagic 6

200 MHz ARM9E core, plus …

Hard-wired accelerators for simple tasks

- BitBlt, color space conversion, scaling, …

"Associative Processing Array" programmable accelerator for complex tasks

- Video, 3-D graphics

Extensive I/O interfaces

- Direct connection to camera sensor, LCD …
- Dedicated interface for baseband processor

Claim: MPEG-4 decode *with post-processing* (simple profile, level 1, QCIF, 15 fps): 13 MHz

Sampling now at $18 (10 ku)

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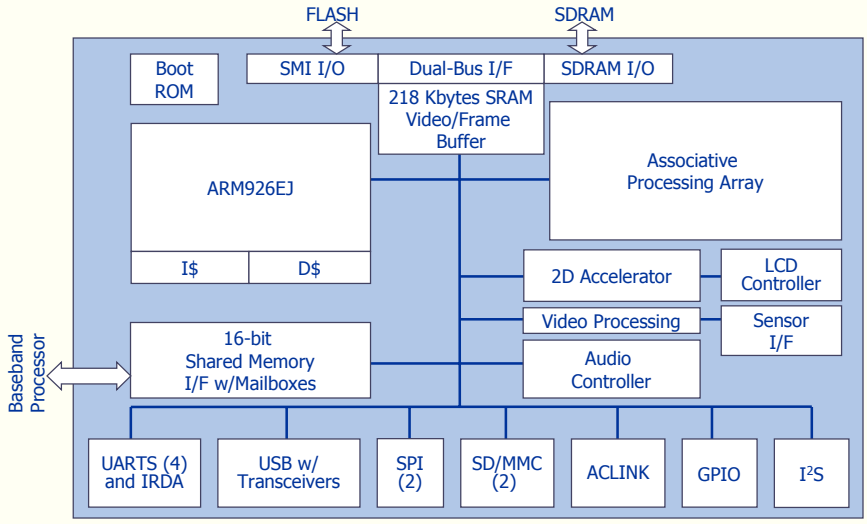
MiMagic 6 On-Chip Integration



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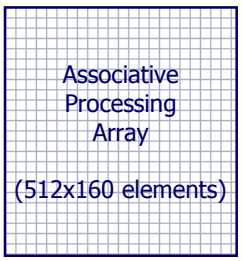
Associative Processing Array

Array of 1-bit memory and processing elements
- Serves as both processing engine and as cache
- First implementation: 512 rows x 160 columns

Operations performed column-wise
- Operations performed on 512 rows in parallel

Only three basic operations: compare, write, move
- Complex operations built up via Boolean logic
- E.g., 8-bit addition requires 25 cycles
  - But can do 512 at once → throughput ~20 per cycle

Common word-wise operations supported via library



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NeoMagic MiMagic 6

Strengths and Weaknesses

- Performance, efficiency unknown
- ↑ Exemplary integration
  - ↑ Designed from the ground up for multimedia
- ↑ APA may deliver excellent energy efficiency
  - ↑ Potential for dramatic reduction in data movement
- ↑ 3D graphics acceleration
- ↑ APA is programmable, and therefore flexible, but …
- ↓ Very unusual, complex programming model
  - ↑ NeoMagic will provide a few key software blocks
  - ↓ For other functions, users must brave a complex architecture with immature tools

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Hard-wired Accelerator(s)

Strengths and Weaknesses

- ↑ Architecture designed for media processing
  - ↑ Potential for excellent speed and energy efficiency
  - ↓ Typically perform only a narrow set of tasks
- ↓ Simple programming model
- ↓ Limited flexibility
- ↓ Little compatibility
- ↓ Limited third-party software component support

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Motorola i.MX21

Based on a 266 MHz ARM9E core

Accelerators for MPEG-4/H.263 encode and decode, video pre- and post-processing

Strong emphasis on energy-saving design

- Accelerators to reduce overall clock speed
- Active well biasing

MPEG-4 decode (simple profile, level 1, QCIF, 15 fps): 3 MHz

Shipping second half of 2004 at $20 (10 ku)

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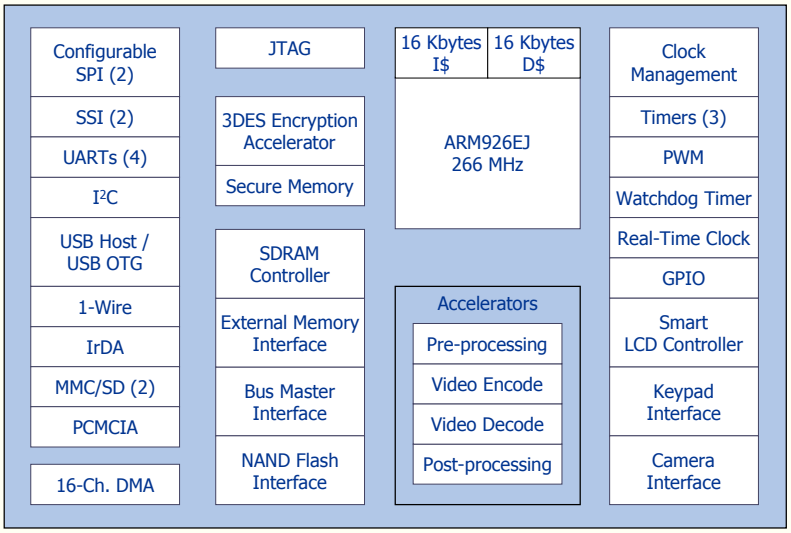
i.MX21 On-Chip Integration



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Motorola i.MX21

Strengths and Weaknesses

- ↑ Potential for good performance, cost-performance
  - ↑ Likely good speed for targeted tasks
- ↑ Potential for good energy-efficiency for some tasks
- ↑ Good peripheral integration
  - ↓ But on-chip memory is limited to small caches
- ↓ All on-chip memories are caches
- ↓ Video encoding/decoding accelerators are inflexible
  - ↑ Post- and pre-processing accelerators are more flexible
- ↑ Simple programming model
- ↑ Vendor has long experience in applications processors

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Applications Processor Trends

New apps move to the fore
- 3D games
- Personal content

Increasing architectural complexity
- Many heterogeneous multiprocessors
- Many specialized coprocessors and accelerators

Flexibility vs. efficiency is a key dilemma

Hardware abstraction increases
- OSs, drivers, APIs …
- Vendor-provided libraries

Integration increasing
- Memory integration particularly important

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Conclusions

Emerging mobile applications make increasingly tough signal-processing demands
- Many architectural approaches can get the job done--but efficiency, ease of development, etc. vary widely
- Serious DSP-oriented features appearing in even low-end processors

Performance comparisons become increasingly difficult as applications converge and architectures diverge
- Independent benchmarking a must

Raw performance is not enough
- Efficiency is key
- Considerations like development infrastructure and vendor roadmap are crucial

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2004 Edition

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